

A 128×128 Pixel 120-dB Dynamic-Range Vision-Sensor Chip for Image Contrast and Orientation Extraction

Pierre-François Rüedi, *Member, IEEE*, Pascal Heim, *Associate Member, IEEE*, François Kaess, *Member, IEEE*, Eric Grenet, Friedrich Heitger, Pierre-Yves Burgi, Stève Gyger, and Pascal Nussbaum

Abstract—A vision sensor for low-cost, fast, and robust vision systems is described. The sensor includes an on-chip analog computation of contrast magnitude and direction of image features. A temporal ordering of this information according to the contrast magnitude is used to reduce the amount of data delivered. This sensor, realized in a 0.5- μm two-poly three-metal technology, features a contrast sensitivity of 2%, a contrast direction precision of $\pm 3^\circ$, and an illumination dynamic range of 120 dB. Applications with uncontrolled lighting conditions are ideal for this sensor.

Index Terms—Analog VLSI, CMOS vision sensor, contrast computation, early vision, orientation computation, temporal coding.

I. INTRODUCTION

THERE IS AN increasing demand for low-cost and compact vision systems performing a fast and reliable analysis of visual scenes, even under extreme lighting conditions. Taken together, these requirements seem difficult to be met by today's conventional image sensing and signal-processing approaches. Particular challenges reside in the problems of extracting only pertinent image features and to achieve a stable feature representation, largely independent on the conditions and variations of lighting.

In general, relevant visual information, such as object contours, is represented by the changes in intensity (spatial gradients) rather than absolute intensity values. Reducing the image information to significant changes in intensity considerably lessens the computational burden for further processing steps. However, the magnitude of local differences in intensity or spatial gradients, if generated by the differential reflection properties of objects, varies in direct proportion with the strength of the illuminant. This renders any extraction of significant spatial gradients inherently unstable. On the other hand, a measure of local contrast does not have this disadvantage, as by normalization it discards the strength of illumination sources. It is obvious that, for representing contrast, the image sensing requires a higher dynamic range to capture the span of scenic intensities.

Manuscript received May 9, 2003; revised June 17, 2003.

P.-F. Rüedi, P. Heim, F. Kaess, E. Grenet, F. Heitger, S. Gyger, and P. Nussbaum are with the Swiss Center for Electronic and Microtechnology, S.A. 2007 Neuchâtel, Switzerland (e-mail: pfr@csem.ch; phe@csem.ch).

P.-Y. Burgi was with the Swiss Center for Electronic and Microtechnology, S.A. 2007 Neuchâtel, Switzerland. He is now with the Information and Communication Technology Group, University of Geneva, 1211 Geneva 4, Switzerland.

Digital Object Identifier 10.1109/JSSC.2003.819169

A fast and efficient implementation can be achieved by shifting part of the signal processing to the pixel itself. A survey of the literature shows a tendency toward this direction [1]–[5].

The vision sensor described in this paper is a step toward fulfilling the following requirements by incorporating essential image-processing operations on the sensor chip:

- 1) auto-exposure at the pixel level introduces a high dynamic range;
- 2) real-time operation is achieved by pixel-parallel analog computation of contrast magnitude and direction;
- 3) post-processing is facilitated by a data communication scheme, which allows to convey only significant image information ordered according to signal magnitude.

In [6], we described a current mode implementation of a vision sensor delivering the spatial gradient magnitude and direction of image features. This paper is an extension to what has been done in [6] by using a voltage-mode implementation to compute the contrast magnitude and direction of image features. The main advantages of this approach are: 1) a contrast representation, discarding the strength of illuminants (the implementation realized in [6] provided only gradients) and 2) a much better accuracy of the device allowing to detect weak contrasts (2%) over a wide range of illumination (120 dB).

The remainder of this paper is organized as follows. Section II describes the principles of operation. In Section III, the implementation is discussed in details. Section IV presents measurement results. Finally, Section V draws conclusions.

II. OPERATIONAL PRINCIPLE

The purpose of the processing performed at the pixel level is to build representations of contrast magnitudes and contrast directions. Contrast direction is a powerful clue for performing recognition operations. Furthermore, the contrast magnitude information is used to temporally dispatch the feature information of each pixel, prioritizing pixels with a strong contrast magnitude. In a visual scene, pixels with a high contrast can be sparse [7], and are mostly associated with important information such as object boundaries [8]. Dispatching information by decreasing order of contrast magnitude has two main advantages: significant information is delivered first and the amount of data dispatched out of the circuit can be reduced to the information needed to perform a given task. Operations performed at the pixel level can be divided in the following successive steps:

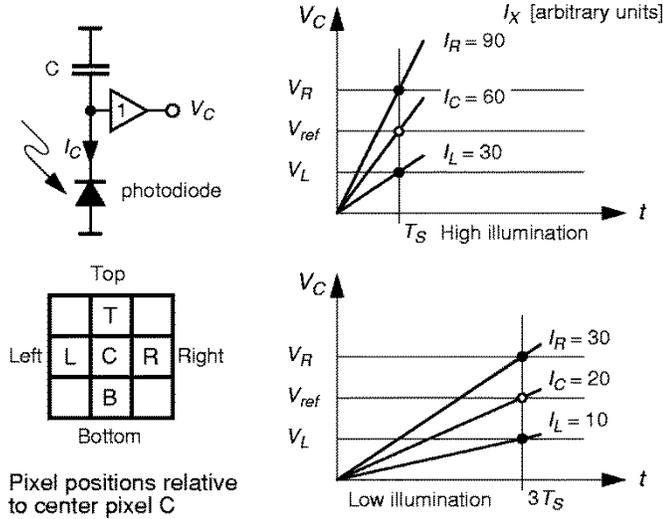


Fig. 1. Contrast generation.

- Step 1) build-up of a contrast representation;
- Step 2) computation of contrast magnitude and direction;
- Step 3) ordered dispatching of this information.

A. Contrast Representation

The traditional approach to acquire an image with a CMOS imager consists of integrating on a capacitor, in each pixel of an array, the photocurrent delivered by a photodiode for a fixed exposure time. Without saturation, the resulting voltages are then proportional to the photocurrents. Here, similarly to [9]–[12], instead of integrating photocurrents for a fixed duration, photocurrents are integrated until a given reference voltage is reached. The principle is illustrated in Fig. 1, where a central pixel and its four neighbors are considered (left, right, top, and bottom). In each pixel, the photocurrent I_C is integrated on a capacitor C . The resulting voltage V_C is continuously compared to a reference voltage V_{ref} . Once V_C reaches V_{ref} , the central pixel samples the voltages V_L , V_R , V_T , and V_B of the four neighboring pixels and stores these voltages on capacitors. The local integration time T_S is given by

$$T_S = \frac{C \cdot V_{ref}}{I_C}. \quad (1)$$

Let I_X be the photocurrent in neighbor X , the sampled voltage will be

$$V_X = \frac{I_X \cdot T_S}{C} = \frac{I_X}{I_C} V_{ref}. \quad (2)$$

Thus, voltage V_X is independent of the illumination level and depends only on the ratio of the photocurrents generated in pixels X and C . With the assumption that the photocurrent of the central pixel corresponds to the average of its four neighbors, which is mostly fulfilled with the spatial low-pass characteristics of the optics, one has

$$I_C = \frac{I_R + I_L}{2} = \frac{I_T + I_B}{2}. \quad (3)$$

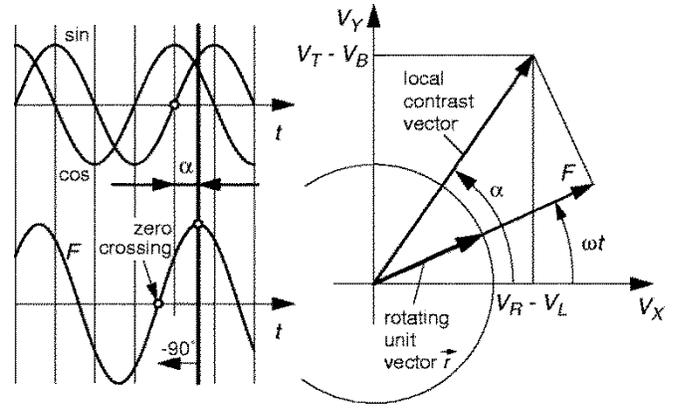


Fig. 2. Computation of contrast magnitude and direction.

Combining (2) and (3) and solving for $V_R - V_L$ gives

$$V_R - V_L = 2 \frac{I_R - I_L}{I_R + I_L} V_{ref}. \quad (4)$$

Similarly, for $V_T - V_B$, one gets

$$V_T - V_B = 2 \frac{I_T - I_B}{I_T + I_B} V_{ref}. \quad (5)$$

Notice that (4) and (5) are equivalent to the definition of the Michelson contrast with the standard notation

$$C = \frac{L_{max} - L_{min}}{L_{max} + L_{min}} \quad (6)$$

where L is the luminance.

Therefore, voltages $V_R - V_L$ and $V_T - V_B$ can be considered the X and Y components of a local contrast vector. These components depend on the relative change of luminance captured by the group of 3×3 pixels, which is independent of the illumination level. If the illumination level is decreased by a factor of three, as illustrated in Fig. 1, the time elapsed between the start of the integration and the sampling of the four neighbors is three times longer so that the sampled voltages remain the same.

B. Computation of Contrast Magnitude and Direction

The computation of the contrast direction and magnitude of the contrast vector defined in (4) and (5) is illustrated in Fig. 2. For each pixel, the projection of the local contrast vector on a rotating unit vector \vec{r} is continuously computed. This projection $F(t)$ is given by

$$F(t) = \frac{\partial V_{i,j}}{\partial r(t)} = \frac{V_R - V_L}{2V_{ref}} \cos \omega t + \frac{V_T - V_B}{2V_{ref}} \sin \omega t \quad (7)$$

where $\cos \omega t$ and $\sin \omega t$ are two steering functions distributed to all pixels in parallel, which correspond to the components of \vec{r} .

When \vec{r} points in the same direction as the local contrast vector, $F(t)$ goes through a maximum. Thus, $F(t)$ is a sine wave whose amplitude and phase represent the magnitude and direction of the contrast vector.

C. Data Output

To illustrate the data output, a frame acquisition and the whole sequence of operations for two pixels a and b is shown in Fig. 3. During a first phase, photocurrents are integrated. The

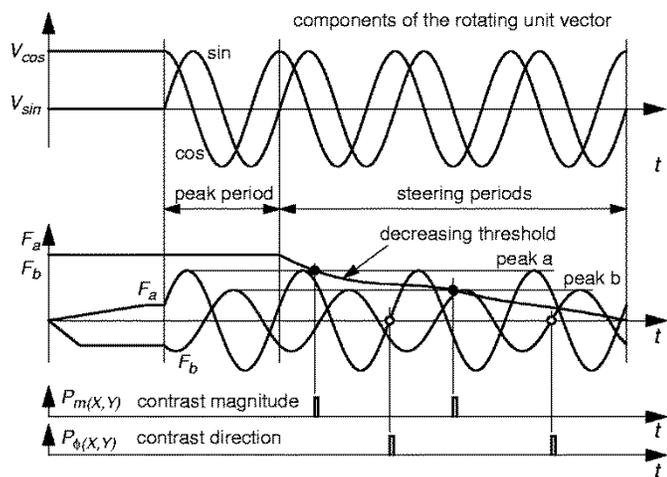


Fig. 3. Data output principle (two pixels a and b are represented).

steering functions are then turned on. During the first steering period, $F_a(t)$ and $F_b(t)$ go through a maximum, which is detected and memorized by a simple maximum detector (peaks a and b). During the subsequent periods, a monotonously decreasing threshold function is distributed to all pixels in parallel. In each pixel, this threshold function is continuously compared to this maximum. To output the contrast magnitude, a pulse encoding the address (X, Y) of the pixel is emitted on a communication bus [13], [14] when the threshold function reaches the maximum of the individual pixel. Thus, the contrast present at each pixel is time encoded, with the high contrasts preceding the lower ones. This scheme allows to limit data transmission to pixels with a contrast higher than a given value by stopping data transmission. To dispatch the contrast direction, a pulse is emitted on the communication bus at the first zero crossing with positive slope that follows. By this, the contrast direction is ordered in time according to the contrast magnitude. Without gating of the contrast direction by the contrast magnitude, each pixel would fire a pulse at the first occurrence of the zero crossing. Notice that the zero crossing is shifted by -90° with respect to the maximum of $F(t)$.

D. Edge Thinning

To further reduce the amount of data transmitted by the sensor, an edge-thinning algorithm, commonly referred to as nonmaximum suppression (NMS), is implemented at the pixel level. The purpose of this algorithm is to keep only the ridge of contrast, reducing edges to a one-pixel width marking. Taking advantage of the temporal ordering of contrast magnitudes leads to a very efficient implementation of this algorithm.

Let us first consider the one-dimensional profile of contrasts represented in Fig. 4. A local maximum of contrast occurs when the left and right neighbors have a lower contrast value than the central pixel. Taking advantage of the temporal ordering of contrast magnitude, the implementation of the NMS algorithm boils down to inhibit the transmission of the feature information in the left and right neighbors. This occurs once the decreasing threshold function becomes lower than the local contrast value. In Fig. 4, inhibition starts from pixel P_4 to propagate in the left

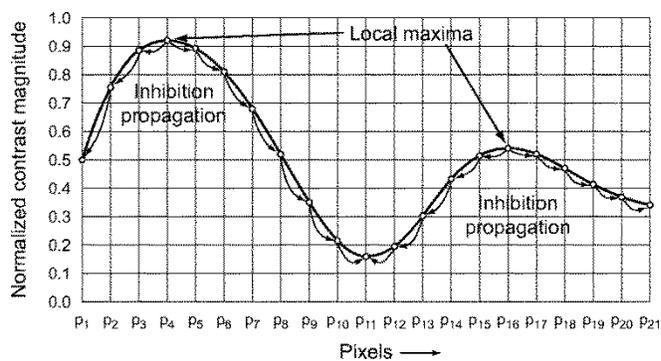


Fig. 4. Principle of the one-dimensional NMS algorithm.

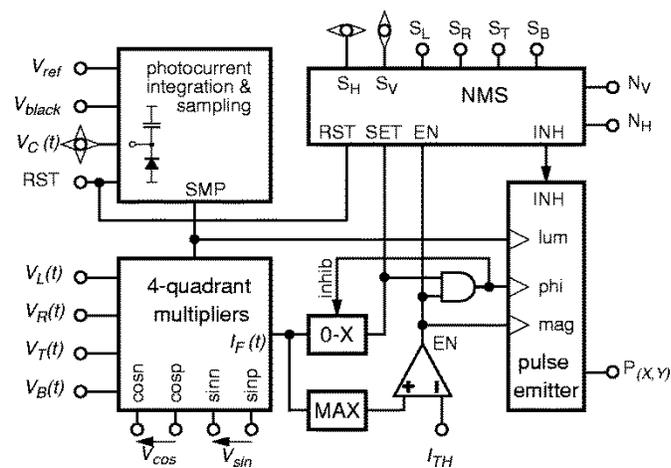


Fig. 5. Block schematic of a pixel.

and right directions as the threshold is decreased. Later, inhibition starts from pixel P_{16} . The two-dimensional implementation of this algorithm requires to inhibit neighboring pixels only in the direction perpendicular to the ridge of contrast. The propagation of inhibition is restricted to the horizontal and vertical directions. For directions of contrast closer to horizontal, the left and right neighbors are inhibited. For directions closer to vertical, the top and bottom ones are inhibited.

III. IMPLEMENTATION

A block diagram of a pixel is illustrated in Fig. 5. The *photocurrent integration and sampling block* integrates the photocurrent on a capacitor, dispatches the resulting voltage V_C to the four neighbors, and compares this voltage to voltage V_{ref} in order to trigger the sampling of voltages V_R , V_L , V_T , and V_B provided by the four neighbors. The *four-quadrant multipliers* block implements the multiplication of these four voltages by a sine and a cosine functions. The output of the multipliers is a current (I_F) representing the function $F(t)$. It is fed to a maximum detector, which detects and holds the maximum of I_F , and to a zero-crossing detector, which emits a pulse at the occurrence of a zero-crossing with a positive slope. The output of the maximum detector is compared with the decreasing global threshold function I_{TH} . Upon matching, signal EN goes high, triggering the emission on a communication bus of a pulse encoding the address of the pixel. The pulse encoding

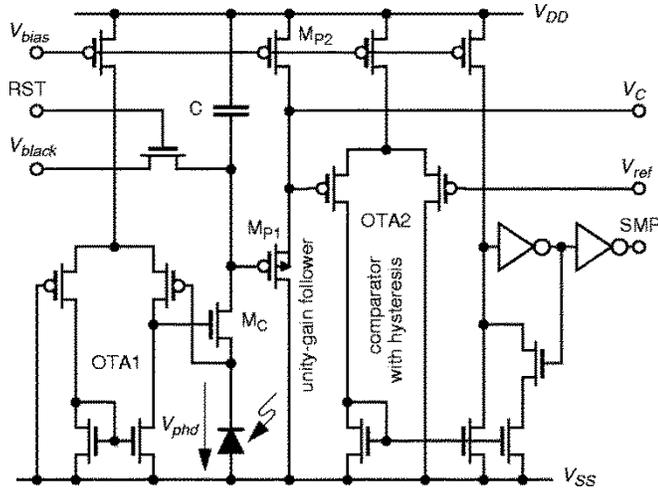


Fig. 6. Circuit schematic of the photocurrent and sampling block.

the contrast direction is emitted at the first zero crossing that follows. Following the emission of the contrast direction pulse, the zero-crossing detector is inhibited to prevent the pixel from sending pulses at each subsequent zero crossing. The *NMS block* inhibits the emission of the contrast magnitude and contrast direction when the local contrast magnitude is not a local maximum. For test purposes, a pulse is emitted on the communication bus simultaneously to the sampling of the four neighbors. As the time when the pulse is emitted is inversely proportional to the photocurrent, this feature offers the possibility to display a gray-level image of the visual scene. The implementation of the maximum detector is described in [6], whereas the zero-crossing detector is described in [6] and [15]. The other blocks are detailed below.

A. Photocurrent Integration and Sampling Block

The function of this block is to generate four voltages independent of the illumination level. Fig. 6 shows the schematic of the photocurrent integration and sampling block. When signal *RST* is high, capacitor *C* is reset to voltage V_{BLACK} . Transistor M_C together with *OTA1* maintain a constant voltage across the photodiode so that the photocurrent is not integrated on the parasitic capacitance of the photodiode. The transconductance amplifier has an asymmetrical input differential pair to generate a voltage V_{phd} around 25 mV. The voltage follower made of *MP1* and *MP2* is a simple p-type source follower in a separate well to get a gain close to one and minimize the parasitic input capacitance. Voltage V_C is distributed to the four neighbors and compared to a reference voltage V_{ref} . At the beginning of the photocurrent integration, signal *SMP* is high. When V_C reaches V_{ref} , signal *SMP*, which is fed to the *four-quadrants multiplier* block, goes down.

B. Analog Multipliers

This block implements the multiplication of the voltages delivered by the neighbor pixels by a sine and a cosine function, as illustrated in Fig. 7. Transistors M_1 – M_8 implement two four-quadrants multipliers operating in strong inversion [16], [17]. At the beginning of a frame acquisition, signal *SMP* is high so that V_L , V_R , V_T , and V_B are applied to the gates of transistors

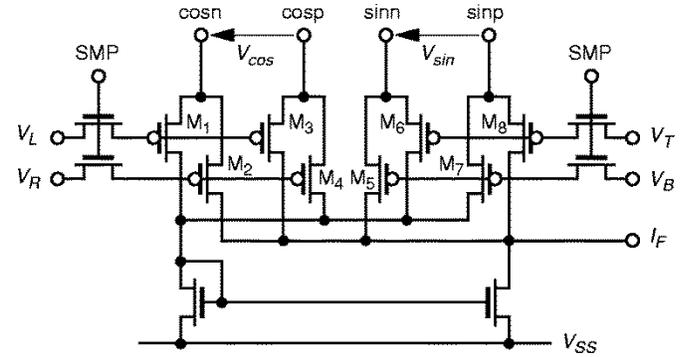


Fig. 7. Circuit schematic of the double analog four-quadrant multiplier.

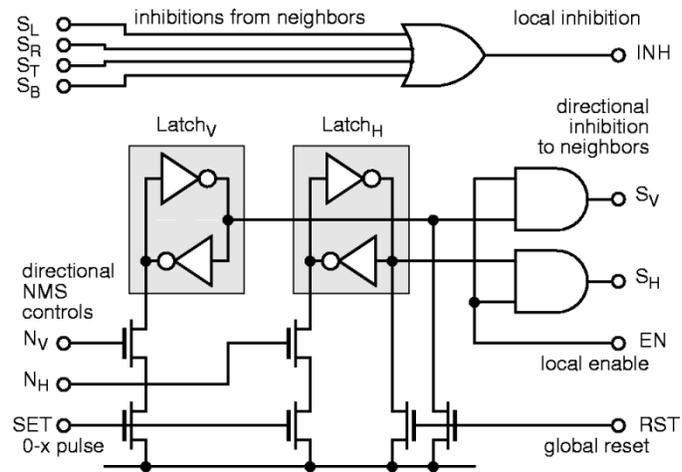


Fig. 8. NMS circuit schematic.

M_1 – M_8 . When signal *SMP* goes low, these four voltages are held on the parasitic gate capacitances of M_1 – M_8 . The signed cosine and sine functions are generated as two differential voltages applied by class-AB amplifiers to the sources of these transistors. The output of the multipliers is the sine current I_F , of which amplitude and phase represent the magnitude and direction of the contrast, respectively.

C. Nonmaximum Suppression Block

Fig. 8 illustrates the schematic of the *NMS block*. The function of this block is to prevent the neighboring pixels in a direction perpendicular to the ridge of contrast from sending their feature information once I_{TH} matches the output of the maximum detector. Prior to the activation of this mechanism, the direction (horizontal or vertical) in which the inhibition must occur has to be determined and stored in each pixel. To this end, signals N_V and N_H are digital signals generated by a control block in relation with the sine and cosine functions to indicate the direction of inhibition corresponding to a given orientation, as illustrated in Fig. 9. These signals are advanced by 90° with respect to the rotating vector to take into account the phase shift between the zero crossing with a positive slope and the orientation of the contrast. At the beginning of a frame acquisition, latches L_V and L_H are reset. During the first steering period, a pulse is triggered on signal *SET* at the zero crossing of I_F to make latches L_V and L_H store the state of signals N_V and N_H . Signals S_V and S_H are inhibition signals, active high, sent

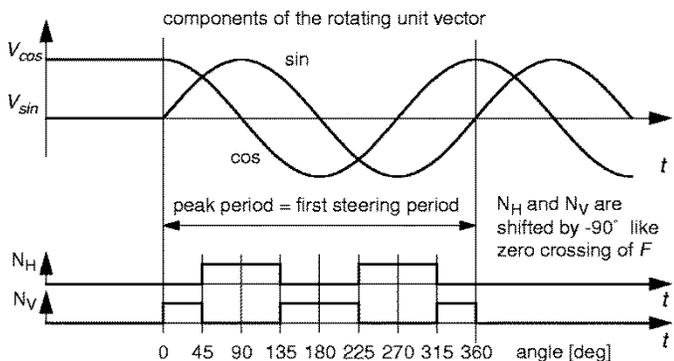


Fig. 9. NMS control signals.

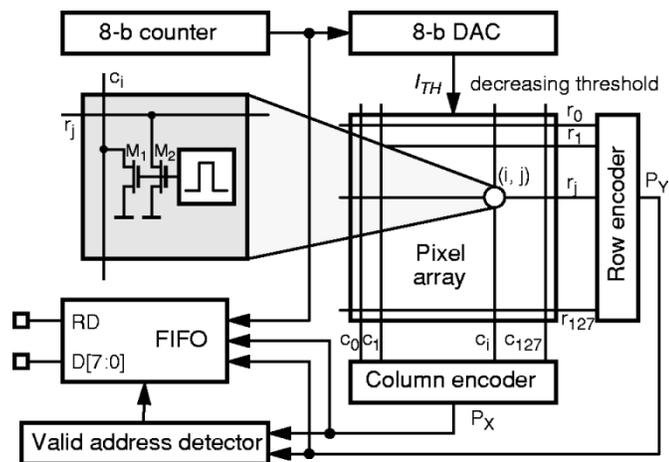


Fig. 10. Data readout architecture.

to the vertical (top and bottom) and horizontal (left and right) neighbors, respectively. Subsequent to the first steering period, signal I_{TH} is monotonously decreased, as described previously. When signal EN goes high, the horizontal or vertical neighbors are inhibited depending on the states of latches L_H and L_V , respectively.

Signals S_L , S_R , S_T , and S_B are inhibition signals received from the left, right, top, and bottom neighboring pixels, respectively. As soon as one of these four signals goes high, the output of the OR gate goes high, disabling the pulse emitter. This prevents the pixel to transmit its feature information. Therefore, a pixel transmits its feature information only if signal I_{TH} matches the output of the maximum detector, before that this event occurs in the neighboring pixels.

D. Data Output

The transmission of contrast magnitude or orientation is illustrated in Fig. 10. A monotonously decreasing threshold function is generated by an 8-bit counter coupled to an 8-bit D/A converter. The threshold function can be either a straight ramp or any arbitrary monotonously decreasing function depending on the clocking of the counter. The resulting signal I_{TH} is distributed to all pixels. Each pixel (i, j) in the array is connected to a horizontal (r_j) and a vertical (c_i) wire crossing the pixel. Upon matching of I_{TH} and $\max(I_F)$, a current pulse is pulled by transistors M1 and M2 on these two wires. Row and column encoders placed on the right and bottom of the pixel array, respec-

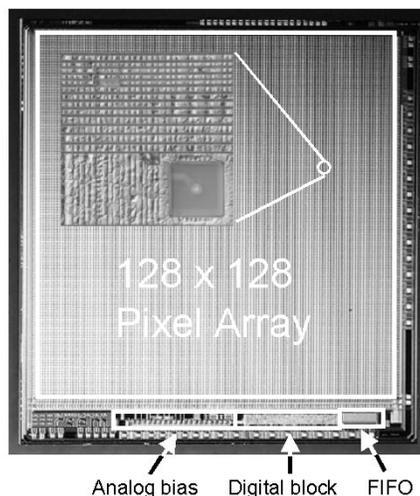


Fig. 11. Micrograph of the circuit.

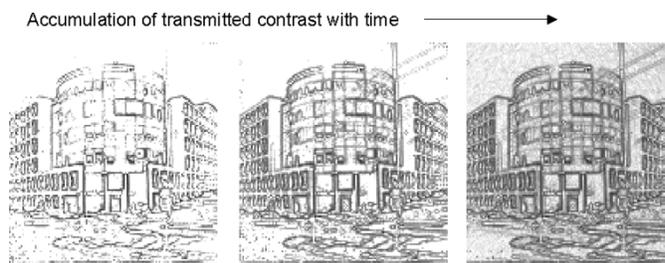


Fig. 12. Temporal dispatching of contrast magnitude information.

tively, perform two functions. First, they maintain these wires at a constant voltage and detect incoming current pulses. Second, upon detection of a current pulse, they generate on P_X and P_Y , a double-rail address encoding the corresponding column and row positions, respectively. The address is encoded by pulling a current for a logical “1”. As pulse emission is asynchronous, collisions of pulses may occur; however, they result in a non-valid double-rail code. The *valid address detection* block detects the occurrence of a valid double-rail address on P_X and P_Y , and triggers the sampling of P_X , P_Y , and the counter state by a first-in-first-out (FIFO) buffer with a capacity of 16 words of 24 bit. The stored information is read through an 8-bit data bus. Transfer of contrast direction information proceeds in a similar manner by sampling in the FIFO the address of a pixel emitting a pulse, together with an 8-bit word coding the phase of the sine and cosine functions.

IV. RESULTS

A circuit containing a 128×128 pixel array has been integrated in a $0.5\text{-}\mu\text{m}$ three-metal two-poly technology. The die micrograph, together with a close-up of a pixel, are illustrated in Fig. 11. The pixel size is $69 \times 69 \mu\text{m}^2$ with a fill factor of 9%. Total circuit area is 99.7 mm^2 .

A. Contrast Magnitude

Fig. 12 illustrates the temporal dispatching of the contrast magnitude information. The representation uses gray levels to encode the contrast magnitude; black for the largest values and



Fig. 13. Contrast representation with high illumination dynamic range.



Fig. 14. Contrast representation with extreme inhomogeneities of illumination (left and center) and very weak contrasts (right).

white for the smallest ones. First, pixels with a high contrast magnitude transmit their information, mainly corresponding here to the edges of the building, then weaker and weaker contrast information is output.

Fig. 13 illustrates the independence of the contrast representation on the illumination levels present in a scene. The left and center figures are two different gray-level representations of the same image acquired by the sensor to illustrate the high dynamic range of illumination in this visual scene. Data have been obtained by accumulation of the luminance information delivered by the sensor in successive frame acquisitions to reduce the effect of the collisions on the communication bus. The right figure depicts the contrast representation output by the sensor. The illumination level is suppressed, thus enabling the sensor to accurately represent contrast information even with high inhomogeneities of the illumination. This point is further illustrated in Fig. 14. In the left image, the sun and cars on the road are simultaneously visible. The middle illustration simultaneously depicts very small shadings on the face of a person and a 60-W lit lamp bulb. Finally, the right image in Fig. 14 shows very small shadings on a hand.

The contrast sensitivity of the sensor was assessed by recording its response to gratings with calibrated contrasts. A contrast of 2% could still be detected.

Fig. 15 illustrates the efficiency of the NMS operation to thin edges down to a 1-pixel-wide marking. The top row depicts contrast magnitude representations output by the sensor when the NMS algorithm is disabled. The bottom row depicts the same visual scene with the NMS algorithm turned on. Contrast magnitude thresholding and NMS algorithm are powerful means to reduce the amount of data output by the sensor. In the two left graphics, pixels with a contrast magnitude higher than 5% have output their information. When the NMS algorithm is disabled, this amounts to 56% of the total number of pixels. Enabling the NMS operation reduced the number of pixels to 23%. In the two right representations, only contrasts higher than 30% are dispatched out of the circuit. This results in 23% of the total number of pixels when the NMS algorithm is turned off, and 11% when it is turned on.

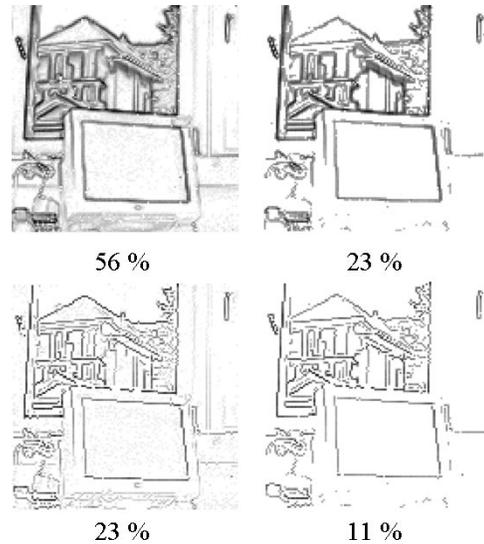


Fig. 15. Efficiency of the NMS algorithm and contrast thresholding to reduce the amount of data transmitted. Top row: without NMS. Bottom row: with NMS. The data output is limited to pixels with a contrast higher than 5% for the left column and 30% for the right column.

B. Contrast Direction

Fig. 16 illustrates the contrast direction representation output by the sensor. Directions of contrast are represented by colors. The left image shows the smooth change of orientation along the bulb of a 60-W lit lamp bulb. The center and right images illustrate the quality of the contrast direction representation of the road. The cars and road markings are clearly visible.

To assess the error on the measurement of the contrast direction, a stimulus made of a straight black-and-gray edge spanning the whole visual field was placed in front of the sensor. Reflectances of both sides of the edge were 4.1% and 9.5%, respectively, corresponding to a contrast of 39.7% between the two surfaces. The optics was slightly defocused to reduce aliasing due to the small fill factor of the pixel (9%), decreasing the pixel-to-pixel contrast to 15%. The NMS operation was turned on in order to limit feature transmission to the contrast ridge. The response of the sensor to different orientations of the stimulus was recorded under an illumination of 680 lux. For each direction, the average and standard deviation of the contrast direction measurements delivered by the sensor were computed. The averaged measured orientation is plotted versus the direction of the stimulus in Fig. 17. The deviation from linearity is illustrated in Fig. 18. The maximum error is 3° . This error is composed of at least three components which are: 1) the estimated tolerance on the stimulus orientation of 0.5° , 2) the remaining error caused by aliasing, which amounts to an estimated 1° – 2° (a solution to reduce the aliasing would be to use micro-lens to increase the fill factor of the pixel and this would also increase the sensitivity of the sensor); and 3) the remaining systematic errors are caused by distortions of the sine and cosine components applied to the multipliers, as well as nonlinearities of the multipliers. These nonidealities are in the range of 1° – 2° . The standard deviation is illustrated in Fig. 19. It ranges from 4.5° to 6.2° without any noticeable relation to the direction of the stimulus.

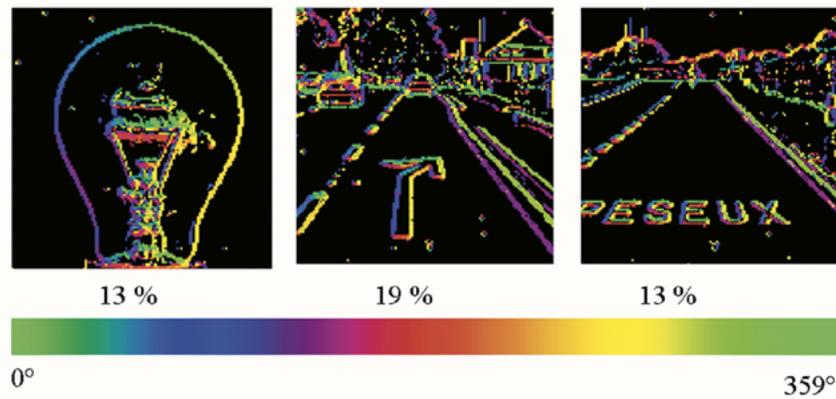


Fig. 16. Contrast direction representation output by the sensor. The number below each image indicates the percentage of pixels that have transmitted their direction of contrast.

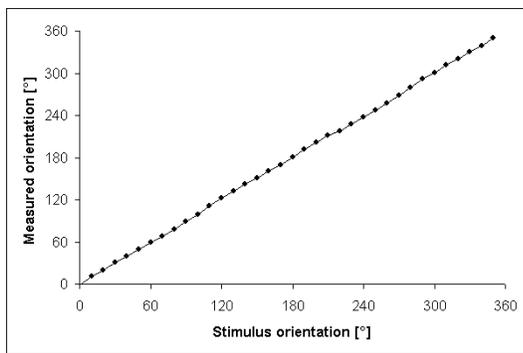


Fig. 17. Measured orientation for different orientations of a black-to-gray edge.

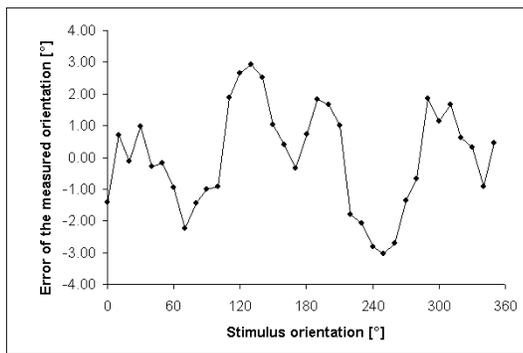


Fig. 18. Error on the measured orientation of a black-to-gray edge.

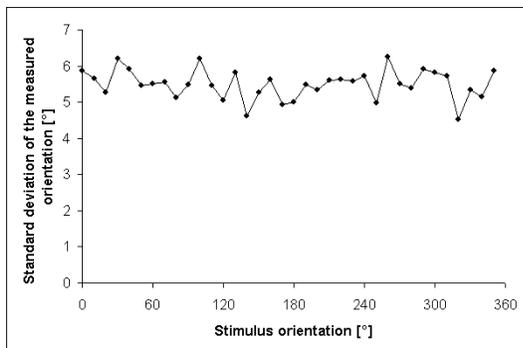


Fig. 19. Standard deviation of the measured orientation of a black-to-gray edge delivered by a population of pixels.

TABLE I
CHARACTERISTICS OF THE CIRCUIT

Technology	0.5 μm , 3 metal, 2 poly
Pixel size / Fill factor	69 × 69 μm^2 / 9 %
Conversion factor	46 $\mu\text{V}/\text{e}^-$
Dark current	0.3 pA at 25 °C
Integration time	0.5 μs ... 15 ms
Integration dynamic range	90 dB
Contrast dynamic range	30 dB
Total dynamic range	120 dB
Data compute and dispatch	2 ms
Frame rate	1/(max integration time + 2 ms)
Contrast sensitivity	2 %
Orientation precision	+/- 3°
Power consumption	300 mW at 3.3 V

C. Other Results

Table I lists the characteristics of the sensor. The maximum integration time due to the dark current is 150 ms at 25°C. The maximum usable integration time is arbitrarily fixed to one-tenth of this value. A contrast sensitivity of 2% is maintained up to a corner integration time of 3 ms, and then decreases to 10% for the maximum integration time of 15 ms. This 2% sensitivity corresponds to a 6-bit or 30-dB increase in the dynamic range of the sensor. The typical data compute and dispatch time is 2 ms. The power consumption is 300 mW.

V. CONCLUSION

A vision sensor that computes at the pixel level the contrast magnitude and direction of image features has been described. As these representations are largely independent of the illumination, this sensor is ideally suited to faithfully capture and reconstitute the important features of environments with high inhomogeneities of illumination. Furthermore, the dispatching of this information is temporally encoded by decreasing order of contrast magnitude. This scheme allows to limit transmission of the feature information to parts of the image with significant contrast magnitude. This results in a strong reduction of the amount

of data delivered by the sensor, which, in turn, reduces the processing power requirements for subsequent processing stages. Work on algorithms exploiting the possibilities and potential of this specific architecture has been ongoing over the last two years and is showing promising results to achieve low-cost and robust vision systems, particularly for automotive and surveillance applications.

REFERENCES

- [1] A. G. Andreou, R. C. Meitzler, K. Strohbahn, and K. A. Boahen, "Analog VLSI neuromorphic image acquisition and pre-processing systems," *Neural Netw.*, vol. 8, pp. 1323–1347, 1995.
- [2] A. Moini, *Vision Chips*. Norwell, MA: Kluwer, 1999.
- [3] B. E. Shi, "A low power orientation selective vision sensor," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 435–440, May 2000.
- [4] B. E. Shi and T. Choi, "A Michelson contrast sensitive silicon retina," in *Proc. 8th Int. Neural Information Processing Conf.*, 2001.
- [5] R. Etienne-Cummings, J. van der Spiegel, and P. Mueller, "A foveated silicon retina for two-dimensional tracking," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 504–517, June 2000.
- [6] M. Barbaro, P.-Y. Burgi, A. Mortara, P. Nussbaum, and F. Heitger, "A 100×100 pixel silicon retina for gradient extraction with steering filter capabilities and temporal output coding," *IEEE J. Solid-State Circuits*, vol. 37, pp. 160–172, Feb. 2002.
- [7] D. J. Field, "What is the goal of sensory coding?," *Neural Comput.*, vol. 6, pp. 559–601, 1994.
- [8] R. M. Balboa and N. M. Grzywacz, "Occlusions and their relationship with the distribution of contrasts in natural images," *Vision Res.*, vol. 40, pp. 2661–2669, 2000.
- [9] T. Lule, H. Keller, M. Wagner, and M. Bohm, "100 000 pixel 120 dB imager in TFA-technology," in *VLSI Circuits Symp.*, 1999, pp. 133–136.
- [10] V. Brajovic and T. Kanade, "A VLSI sorting image sensor: Global massively parallel intensity-to-time processing for low-latency adaptive vision," *IEEE Trans. Robot. Automat.*, vol. 15, pp. 67–75, Feb. 1999.
- [11] E. Culuricello, R. Etienne-Cummings, and K. A. Boahen, "A biomorphic digital image sensor," *IEEE J. Solid-State Circuits*, vol. 38, pp. 281–294, Feb. 2003.
- [12] L. G. McIlrath, "A low-power low-noise ultrawide-dynamic-range CMOS imager with pixel-parallel A/D conversion," *IEEE J. Solid-State Circuits*, vol. 36, pp. 846–853, May 2001.
- [13] A. Mortara, E. A. Vittoz, and P. Venier, "A communication scheme for analog VLSI perceptive systems," *IEEE J. Solid-State Circuits*, vol. 30, pp. 660–669, June 1995.
- [14] K. A. Boahen, "Communicating neuronal ensembles between neuromorphic chips," in *Neuromorphic Systems Engineering*, T. S. Lande, Ed. Boston, MA: Kluwer, 1998, ch. 11, pp. 229–261.
- [15] A. Rodriguez-Vasquez, R. Dominguez-Castro, F. Medeiro, and M. Delgado-Restituto, "High-resolution current comparators: Design and application to current-mode function generation," *Analog Integrated Circuits and Signal Processing*, vol. 7, pp. 149–164, 1995.
- [16] K. Bult, "Analog CMOS square-law circuits," Ph.D. dissertation, Univ. Twente, Twente, The Netherlands, 1988.
- [17] S. I. Liu and C. C. Chang, "Low-voltage CMOS four-quadrant multiplier," *Electron. Lett.*, vol. 33, no. 3, 1997.



Pierre-François Rüedi (M'01) was born in Lausanne, Switzerland, in 1965. He received the M.S. degree in microtechnology from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1990.

From 1990 to 1992, he was a Research and Development Engineer with Seiko Instruments, Matsudo, Japan, where he was involved in the design and characterization of SRAM memories. Since 1992, he has been with the Swiss Centre for Electronic and Microtechnology (CSEM), Neuchâtel, Switzerland,

where he is currently a Project Manager with the Advanced Microelectronics Division. His research interests include analog- and mixed-mode design of optical sensors.



Pascal Heim (S'88–A'95) was born in Lausanne, Switzerland, in 1962. He received the B.S.E.E. degree from the Ecole d'Ingénieurs de Genève, Geneva, Switzerland, in 1982, and the M.S.E.E. degree and Ph.D. degree (on the subject of CMOS analog implementations of artificial neural networks) from the Swiss Federal Institute of Technology (EPFL) in Lausanne, Switzerland, in 1989 and 1993, respectively.

In 1994, he joined the group of Prof. M. Jabri at the University of Sydney, Sydney, Australia. In 1995, he joined the Bio-Inspired Group, Swiss Center for Electronics and Microtechnology (CSEM), Neuchâtel, Switzerland, where he has been involved with various types of special optical-sensor chips requiring very dense circuit layouts. Most of these chips are currently used in commercial products.

Dr. Heim was the recipient of a University of Sydney Post-Doctoral Fellowship on analog implementations of weight-perturbation algorithms for multi-layer perceptrons.



François Kaess (S'98–M'02) was born in Strasbourg, France, in 1970. He received the M.S. degree in electrical engineering from Supélec, Gif-sur-Yvette, France, in 1993, and the Ph.D. degree from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 1999.

From 1994 to 1999, he was a Research Assistant with the Electronics Laboratory, Swiss Federal Institute of Technology, where he was involved in the field of GaAs analog-to-digital converters. In 1999, he joined the Bio-Inspired Systems Section, Swiss Center for Electronics and Microtechnology (CSEM), Neuchâtel, Switzerland, where he is involved in the design and exploitation of optical sensors and vision systems.



Eric Grenet was born in Paris, France, on June 9, 1974. He received the Electrical Engineer degree in microelectronics from the Institut Supérieur d'Electronique du Nord (ISEN), Lille, France, in 1998.

He is currently a Research And Development Engineer with the Swiss Center for Electronics and Microtechnology (CSEM), Neuchâtel, Switzerland, where he is involved with bio-inspired microelectronics systems. His research interests include the design of analog circuits in vision-sensor systems and the development of dedicated algorithms in

computer vision.



Friedrich Heitger received the B.S. degree in physics, mathematics, and biology from the University of Toronto, Toronto, ON, Canada, in 1977, and the Master's degree in bio-mathematical psychology and Ph.D. degree in psychophysics from the University of Zürich, Zürich, Switzerland, in 1983 and 1986, respectively. He also completed the nonclinical part of medical school at the University of Freiburg, Freiburg, Germany, in 1986.

From 1987 to 1995, he performed research with the Federal Institute of Technology, Zürich, Switzerland, where he was involved in the field of computer vision and modeling of the visual cortex. Since 1996, he has headed a group in bio-inspired systems design at the Swiss Center for Electronics and Microtechnology, Neuchâtel, Switzerland. His research interests are sensory information processing approaches implemented on analog mixed-mode VLSI circuits.



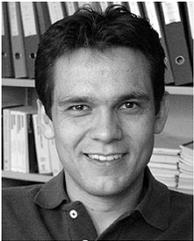
Pierre-Yves Burgi received the B.S. degree in computer engineering from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 1986, and the Ph.D. degree in computer science from the University of Geneva, Geneva, Switzerland, in 1992.

His doctoral studies were followed by a five-year post-doctoral period in visual neurosciences with the Smith-Kettlewell Eye Research Institute, San Francisco, CA, and with the Paul Sabatier University, Toulouse, France. From 1997 to 2003, he was with the Advanced Microelectronics Division, Swiss Center for Electronics and Microtechnology, Neuchâtel, Switzerland, where he conducted research on time-domain processing of visual information for the development of fast silicon vision systems. Since June 2003, he has headed the Information and Communication Technology Group, University of Geneva.



Pascal Nussbaum received the Diploma degree in electronic engineering from the Engineering School of Neuchâtel, Neuchâtel, Switzerland, in 1990.

From 1990 to 1994, he was with the Swiss Center for Electronic and Microtechnology (CSEM), Neuchâtel, Switzerland, where he was involved with analog design CAO tools. In 1994, he joined the Advanced Microelectronics Division, CSEM, to concentrate on self-reconfiguring VLSI in the fault-tolerance domain. In 1998, he joined F. Heitger's group, where he contributed to initiate the steering filters sensors approach, and their exploitation inside vision systems.



Stève Gyger was born in Switzerland, on March 5, 1974. He received the H.E.S. degree in electrical engineering from University of Applied Sciences, Le Locle, Switzerland, in 1996.

He is currently a Research and Development Engineer with the Advanced Microelectronics Department, Swiss Center for Electronic and Microtechnology (CSEM), Neuchâtel, Switzerland. His current research interests include artificial vision, digital ASIC design and mixed-mode VLSI systems.