

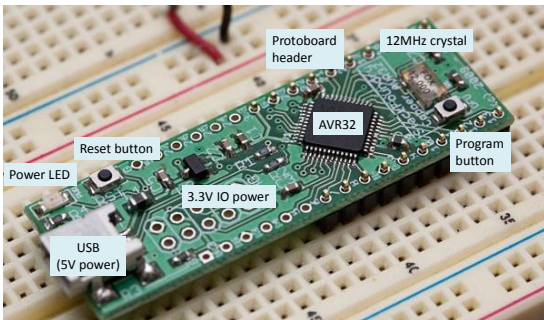
ETH Course 402-0248-00L: Electronics for Physicists II (Digital)

- 1: Setup uC tools, introduction
- 2: Solder SMD AVR32 board
- 3: **Build application around AVR32**
- 4: Design your own PCB schematic
- 5: Place and route your PCB
- 6: Start logic design with FPGAs

The AVR32 AT32UC3B1256

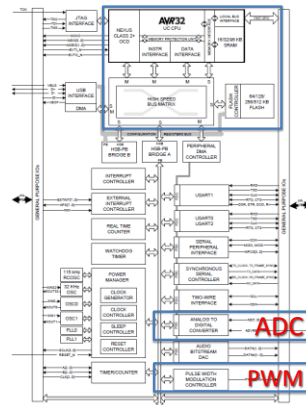
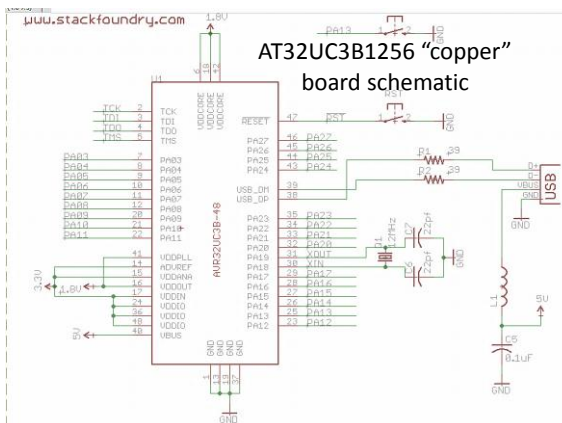
- AT = Atmel: Big microcontroller company
- 32 = 32 bit architecture
- UC3 = Atmel microcontroller family
- B = more powerful and expensive variant (\$7 each @25 units)
- 1 = revision
- 256 = 256kB internal high speed flash memory (32kB single cycle SRAM)

The "bronze" board

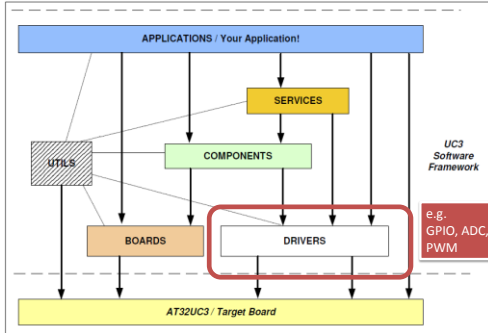


AVR32 capabilities (Ex. 3)

- **System Functions**
 - Power and Clock Manager
 - Two Multipurpose Oscillators
 - Watchdog Timer, Real-Time Clock Timer
- **Interrupt Controller**
 - Auto-vectored Low Latency Interrupt Service with Programmable Priority
- **Universal Serial Bus (USB)**
 - Device 2.0 Full Speed (12Mbps~1Mbps)
- **One Three-Channel 16-bit Timer/Counter (TC)**
- **One 7-Channel 20-bit Pulse Width Modulation Controller (PWM)**
- **Three Universal Synchronous/Asynchronous Receiver/Transmitters (USART)**
- **One Master/Slave Serial Peripheral Interfaces (SPI) with Chip Select Signals**
- **One 8-channel 10-bit Analog-To-Digital Converter, 384ks/s**



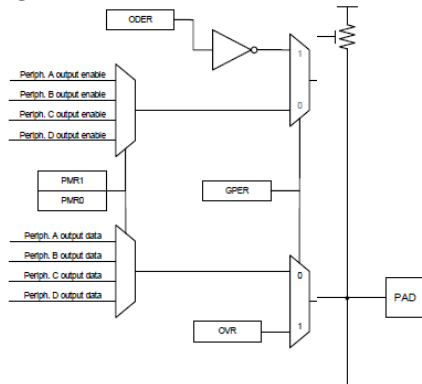
AVR32 Software Framework



“Registers” are memory locations that control or report hardware state

- Example: the PWM registers control everything about PWM, such as period, duty cycle, etc.
- Example: The GPIO (General Purpose Input Output) registers control the pins, such as whether the pin is an *output* (digital 0 or 1) or *input* (high impedance). If the pin is an input, another register controls if a pull-up resistor is enabled.

Figure 17-2. Overview of the GPIO Pac



- 17. General-Purpose Input/Output Controller (GPIO)
 - 17.1 Features
 - 17.2 Overview
 - 17.3 Block Diagram
 - 17.4 Product Dependencies
 - 17.5 Functional Description
 - 17.6 User Interface
 - 17.6.1 Access Types
 - 17.6.2 Enable Register
 - 17.6.3 Peripheral Mux Register 0
 - 17.6.4 Peripheral Mux Register 1
 - 17.6.5 Output Driver Enable Register
 - 17.6.6 Output Value Register
 - 17.6.7 Pin Value Register
 - 17.6.8 Pull-up Enable Register

From the AVR32 datasheet – GPIO registers

ODER
OVR
PUER

ODER register example

17.6.5 Output Driver Enable Register

Name: ODER
Access Type: Read, Write, Set, Clear, Toggle
Offset: 0x40, 0x44, 0x48, 0x4C
Reset Value: -

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- P0-31: Output Driver Enable
 - 0: The output driver is disabled for the corresponding pin.
 - 1: The output driver is enabled for the corresponding pin.

All register have a default reset value

Table 17-4. Register Reset Values

Port	Register	Reset Value
0	GPER	0xFFFFFFFF
0	PMR0	0x00000000
0	PMR1	0x00000000
0	ODER	0x00000000
0	OVR	0x00000000
0	PUER	0x00000000

On reset, all output drivers are disabled

Exercise 3: "Sound volume robot"

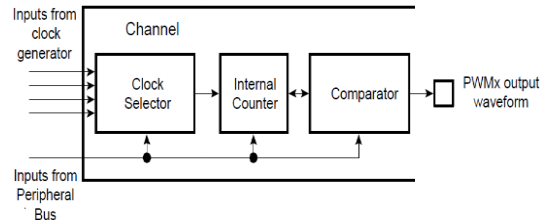
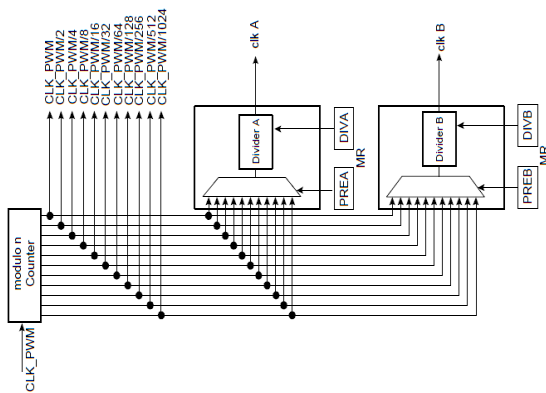
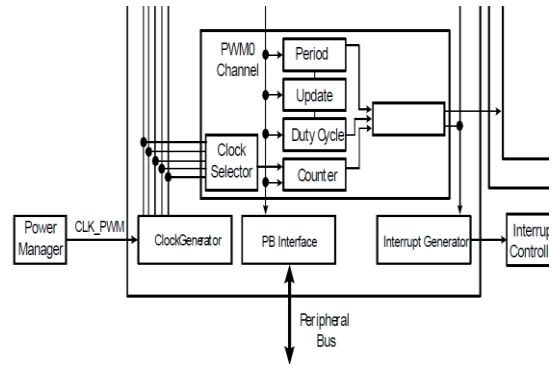
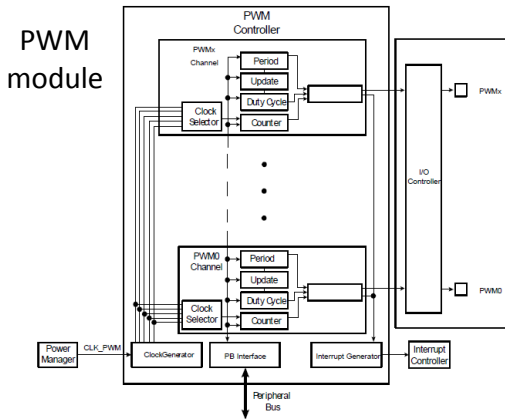
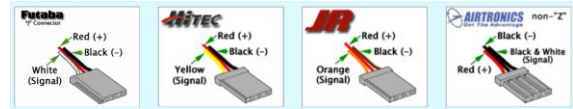
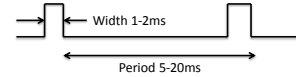
- measures sound volume and moves arm to indicate loudness
- microphone -> preamp -> ADC -> UC -> PWM output



"RC" servos (Radio-Control Servo-Motors)



- Position controlled – Servo has internal position measurement and controller
- Rotation angle 120 degrees
- Pulse width from 1-2ms sets desired position
- Pulses must be sent at frequency 50-200Hz
- Pulse height >2V

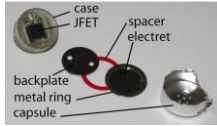
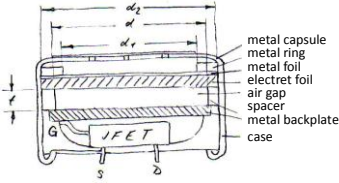


Timing registers

- Period – counter is reset after *cpd*
- Duty Cycle – waveform switches after *cdty*
- Update – *cpd* or *cdty* is updated from *cpd*, depending on *cpd*

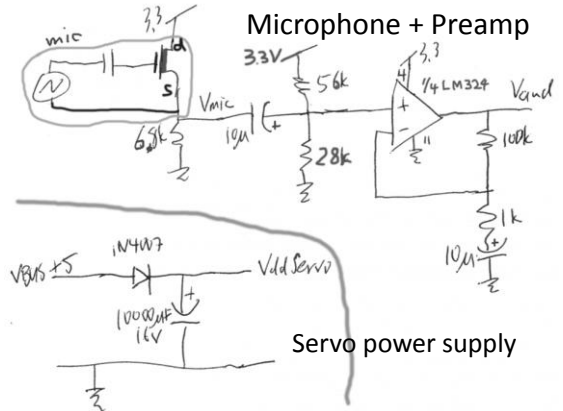
Electret Microphone

- Cheap (< 1\$)
- Electret material, no polarization voltage is required
- Low-noise JFET buffer
- Metal foil is connected to source of the JFET through metal capsule

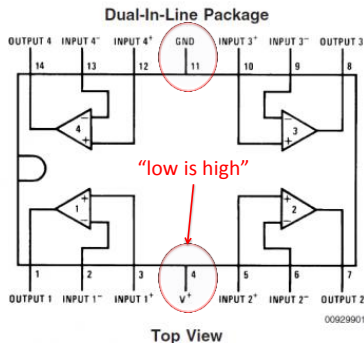


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Microphone + Preamp



LM324 quad JFET opamp



AVR32 Analog to Digital converter

- 10-bit Successive approximation register (SAR) type
- 6 multiplexed single-ended input channels
- Max combined sample rate 384ks/s
- External trigger
- Hardware sequencer
- Peripheral DMA

