

# Addressable Current Reference Array with 170dB Dynamic Range

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## ABSTRACT

Configurable high-performance bias current reference circuits are useful in complex mixed-signal chips. This paper presents the design of a configurable current reference array with ultra wide dynamic range (DR). A coarse-fine architecture using octal coarse current spacing and 8 bits of fine resolution increases the overall current DR with less area compared with the prior work. Compact current multipliers and dividers also save chip areas. Shifted-source current mirrors and an off-current suppression technique improve the accuracy of generated low currents. A buffer with dual-threshold source followers is used to generate the output biasing voltage with a wide DR input current. Biases are individually addressable and configurable. Measurement results of this design in UMC 0.18 $\mu\text{m}$  1P6M CMOS process suggest that over 170dB DR is achieved at room temperature. Each additional bias occupies an incremental area of  $360 \times 22 \mu\text{m}^2$ , which is smaller by a factor of 4 compared to the previous design.

## 1. INTRODUCTION

Configurable current references (biases) are desirable in many mixed-signal circuit designs such as bio-inspired neuromorphic vision sensors [1] and auditory sensors [2], to properly bias different modules with wide current range requirements spanning from strong inversion to below transistors' leakage currents. Since 2005 we have been developing open-source bias generator design kits that can be used to easily incorporate configurable biases onto chips [3,4,12]. Our previous design [4] implemented biases with 32 configuration bits. It used shifted-source current mirrors to enable sub-off current copying ability [10], and thus increased the effective current dynamic range (DR). This capability will become increasingly important as subthreshold leakage increases. However, the reference array was not addressable because all the shift registers (SRs) for digital configuration were connected in series; i.e. to reprogram one bias, the whole SR chain needs to be rewritten even though other biases are unchanged. Each bias achieved 110dB dynamic range with constant 22-bit precision; however, for large current values, such high precision adjustment is not necessary. Rather, what is generally needed is a nominal bias current, and the ability to vary this current around the nominal value with reasonable precision. The nominal current can span orders of magnitude.

This paper describes an improved design of a configurable current reference array. Each bias is individually addressable with the benefit of avoiding SRs

in the array, which saves both programming time and chip area. The 15 configuration bits of each bias are used to program the coarse-fine current selection and the voltage buffer. 3 bits are allocated for coarse current selection, and 8 bits for fine current selection. The current precision (LSB) within each current range is determined by the coarse current values (MSB) and 8-bit binary-weighted division. The remaining 4 bits for buffer configuration have the same functions as described in [4].

In the rest of this paper, we first introduce the overall architecture of the current reference array. We then describe in detail the novel circuit implementations of some crucial parts of the system. We conclude with simulation results and discussion.

## 2. ARCHITECTURE

Fig. 1 shows the overall architecture of the current reference array and the timing diagram. The address and data signals are selected by ADSEL. To program one bias, the address SR is selected and 6 bits of address are input to the address SR using the clock CLK and the data input BITIN. After an address-latch pulse on ALATCH, the address bits are stored in latches and decoded by a 6-to-64 decoder, and accordingly one bias is selected. Next, the data SR is selected and 15 configuration bits are fed into the data SR. After a data-latch pulse on DLATCH, the data bits are stored in the latches of the selected bias, e.g.

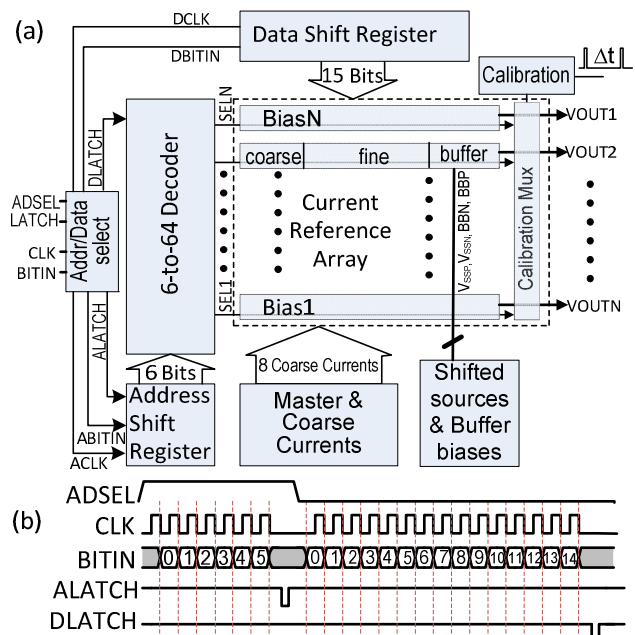


Fig. 1. (a) Architecture of the current reference array and (b) digital signal timing diagram.

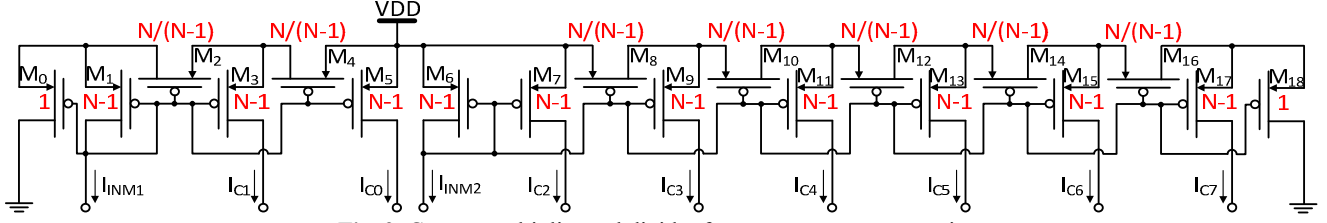


Fig. 2. Current multiplier and divider for coarse current generation.

Bias1. New data can be loaded into the data SR without changing the address. At a clock frequency of 100 kHz, new values can be written in <200us which is much shorter than the several ms in typical previous designs with 30 biases. Removing the SRs from the array should also reduce digital noise during configuration.

The 8 coarse currents derived from the master current are distributed to each bias, and the fine current derived from the one selected coarse current is input to the buffer, where it generates an output biasing voltage  $V_{OUTi}$  ( $i=1\sim N$ ,  $N\leq 64$ ). Shifted sources as in [4] are used for sub-off current biases [10] and they share adjustable regulated voltages for source biasing.

Selected biases are measured via the Calibration Mux either using test transistors as in [4] or by using an integrate-and-fire neuron circuit in the Calibration block, according to its linear current-firing rate relationship. We intend to calibrate biases by connecting this digital output of the neuron to the input of an attached microcontroller counter-timer and adopting methods such as the one described in [11].

### 3. CIRCUIT IMPLEMENTATION

The master current is obtained from the well-known PTAT current reference circuit using weak-inversion MOS transistors and one external resistor [4,5]. It is then multiplied and divided to generate 8 currents for coarse selection. The all-MOS compact circuit for current multiplication and division (Fig. 2) is based on the principle of current division [6]. The ideal normalized width/length ratios of each transistor are marked in red. PMOS transistors are shielded with metals to reduce the influence of photon induced carriers, especially for the smallest currents [3].  $I_{INM1}$  and  $I_{INM2}$  are 1:1 copies of the master current, and the generated coarse currents  $I_{C0}\sim I_{C7}$  have the following relations assuming first-order square

and exponential laws for long channel transistors in strong and weak inversion respectively:

$$\begin{aligned} I_{INM1} &= I_{INM2} = N^{-2}I_{C0} = N^{-1}I_{C1} = N^0I_{C2} = N^1I_{C3} \\ &= N^2I_{C4} = N^3I_{C5} = N^4I_{C6} = N^5I_{C7} \end{aligned}$$

To save chip area, the dimension ratio  $N/(N-1)$  is replaced by 1, the same size as the terminal transistors  $M_0$  and  $M_{18}$ . Then the current scaling ratio is  $N+1-\Delta$  ( $0\leq\Delta<1$ ) instead of  $N$ . Approximate octal weight among  $I_{C0}\sim I_{C7}$  can be achieved by choosing  $N=7$  or  $7.5$ . The  $N=7.5$  is chosen for larger scaling and is implemented as a 13:2 unit transistor ratio (e.g. the ratio between  $M_3$  and  $M_4$ ). The adopted topology saves considerable chip areas compared to conventional current mirror implementations [7], especially for such ultra-wide current value spread.

The 8 coarse currents are copied to each bias by NMOS current mirrors, and 1 of 8 is selected by a 3-to-8 decoder for further division. To deal with large coarse current spread (over 120dB), and to minimize mismatch of current copying among different biases, current mirrors with various and relatively large transistor sizes are used for different coarse currents, so that their over-drive voltages can be maintained at a reasonably high level [8]. Special attention is given to the coarse selection switches for the sake of copying accuracy of the small coarse currents like  $I_{C6}$  or  $I_{C7}$ . Fig. 3(a) shows a conventional current selection scheme using NMOS transistors as selection switches. When the copy of  $I_{C7}$  is selected,  $S_{LSB}$  is closed, and all the other 7 switches are open. Take  $S_{MSB}$  as an example. Its gate and source voltages are grounded, and its drain voltage  $V_C$  is close to  $V_{DD}$  when  $I_{Ci}$ , the selected coarse current, is in the range of  $I_{C7}$ . Although the gate-source voltage  $V_{GS}$  is 0V, its drain-source voltage  $V_{DS}$  is quite large and thus the leakage current could be as large as in the order of tens of pA. The sum of the leakage currents from all the 7 open switches completely overwhelms  $I_{C7}$ . Longer channels would reduce leakage currents, but they still vary considerably with temperature and process corners. Moreover the impedance of the closed switch and the voltage drop across it might be unacceptably large for large coarse currents. To circumvent this problem, additional switches are added as shown in Fig. 3(b). The configuration of open  $S_{0MSB}$ , open  $S_{1MSB}$  and closed  $S_{2MSB}$  elevates the source voltage of  $S_{0MSB}$  to  $V_{DD}$  so that its  $V_{GS}$  is  $-V_{DD}$ , and  $V_{DS}$  is consequently much smaller. Therefore, the leakage currents contributed by  $S_{0MSB}$  and other open switches are

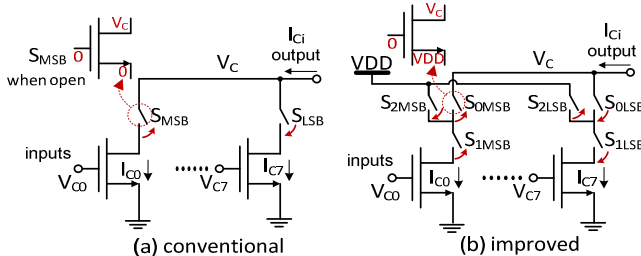


Fig. 3. (a) Conventional current selection scheme. (b) current selection with off-current suppression.

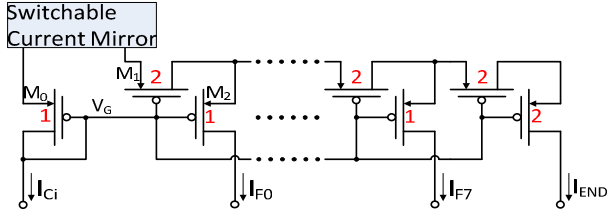


Fig. 4. Current divider for 8 fine currents.

largely suppressed under various process and temperature corners, and  $I_{C_i}$  is a more accurate copy of  $I_{C_7}$ .

The selected coarse current  $I_{C_i}$  is then divided by the R-2R resistor-ladder-like all-PMOS current divider [3,4] to make 8 binary-weighted fine currents  $I_{F0-F7}$  (Fig. 4). The major modification compared to previous designs is that the gate voltage for the PMOS transistors in the divider is not from the fixed gate voltage  $V_{GN}$  of the NMOS transistors in the PTAT current reference circuit; instead, it is provided by the diode-connected  $M_0$ ,  $V_G$ , so that it variably tracks the value of coarse current  $I_{C_i}$ . The current mirror in the gray box is switchable between two transistor pairs with different sizes in order to accommodate the large spread of  $I_{C_i}$ . This cascode structure benefits more accurate current copying and also dividing because low  $V_{GN}$  may cause all PMOS transistors to enter triode region whereas normal current dividing requires the vertical transistors with nominal dimension of 1 to work in saturation region.

The 8 fine currents in each bias are selected in configurable combination by switches, and the sum  $I_{INF}$  of the selected currents is injected into the buffer, shown in Fig. 5, to generate a bias voltage  $V_{OUT}$  to bias other circuit modules, such as pixels, as current mirror pairs. The complicated switching scheme is employed to handle the large span of  $I_{INF}$ . The new features of this buffer circuit compared to the previous version include:

1. The source follower transistors  $M_2$  and  $M_3$ , and  $M_8$  and  $M_9$  are selected by complementary logic output  $S_3$  and  $\bar{S}_3$ ; Normal threshold transistors  $M_3$  and  $M_9$  are connected when  $I_{INF}$  is in the lower range to make sure  $M_0$  and  $M_6$  work in saturation region; low threshold transistors  $M_2$  and  $M_8$  are connected when  $I_{INF}$  is in the upper range to alleviate the supply voltage headroom problem, thanks to the negative gate-source voltage  $V_{GS}$  of NMOS  $M_2$  and the positive  $V_{GS}$  of PMOS  $M_8$ . It is also possible to adjust the  $V_{GS}$  of the source-follower transistors by changing the biasing currents  $I_{BN}$  and  $I_{BP}$ , but much less effectively.

2. The cascode current mirror composed of  $M_0$ ,  $M_1$ ,  $M_4$  and  $M_5$  mitigates the influence of channel length modulation and provides more accurate current copying when the P-type output is enabled;

3. Combinational logic circuits are added to control the switches with inputs from 4 configuration bits and 3 coarse selection bits, ensuring correct functions within wide range of  $I_{INF}$ . For example, when the selected coarse

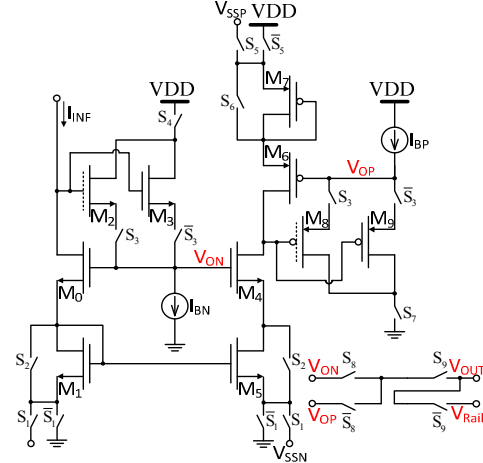


Fig. 5 Configurable buffer circuit to generate the output biasing voltage in each bias. The gates of low threshold transistors are drawn in dashed lines.

current is the largest  $I_{C_0}$ ,  $S_2$  is always closed to disable the cascode transistor  $M_1$  to avoid the headroom problem, regardless of the specific cascode configuration bit; while with other coarse currents selected,  $S_2$  is independently controllable only if  $V_{ON}$  is selected to output, and otherwise  $S_2$  is always open to enable the cascode current mirror.

The output voltage  $V_{OUT}$  can be selected among  $V_{ON}$ ,  $V_{OP}$ , or weakly, through a long transistor, tied to VDD or ground.  $V_{Rail}$  is hard-wired to either VDD or ground in layout and is supplied in reset to ensure correct startup behavior before configuration is loaded. Adjustable shifted-source regulated voltages  $V_{SSN}$  and  $V_{SSP}$  for sub-off current copying and source follower biasing currents  $I_{BN}$  and  $I_{BP}$  are also generated on-chip [4].

#### 4. SIMULATION & MEASUREMENT RESULTS

The array was sent to fabrication in late July in the UMC RF/MM 0.18 $\mu\text{m}$  1P6M CMOS process as part of an event-based asynchronous vision sensor. Fig.6 shows the layout. Each bias occupies area of 360 $\times$ 22 $\mu\text{m}^2$ . The system was simulated using Tanner EDA T-Spice v15.0 with BSIM 3v3 models.

The master current at room temperature is 387nA with a 100k $\Omega$  external resistor. The simulated values and the precision (LSB value) of the 8 coarse currents recorded from  $I_{INF}$  are listed in Table 1. The nominal dynamic range

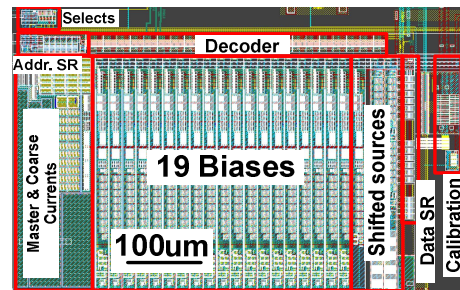


Fig. 6. Layout of the current reference array.

is thus calculated as  $20\log_{10}(24.8\mu/55.72f) \approx 173\text{dB}$ . The scaling ratios between neighboring coarse currents are all close to 8. They are slightly smaller than the calculated values due to secondary effects such as channel-length modulation.

**Table 1.** Simulated values and precisions of the 8 coarse currents at 25°C, and calculated nonlinearities within each current range.

Current	$I_{C0}$	$I_{C1}$	$I_{C2}$	$I_{C3}$
Code	111	110	101	100
Value(A)	24.8 $\mu$	3.16 $\mu$	388n	49.7n
LSB(A)	97.01n	13.34n	1.647n	202.5p
Current	$I_{C4}$	$I_{C5}$	$I_{C6}$	$I_{C7}$
Code	011	010	001	000
Value(A)	6.39n	821p	105p	13.4p
LSB(A)	25.21p	3.198p	409.9f	55.72f

The measured master current is about 390nA, which is consistent with the simulation. Fig. 7 shows the measured current tuning graph with coarse selection codes denoted along with each curve. The smallest 3 coarse ranges are measured using shifted-source biasing. The specific current (current at threshold) and leakage current levels for a  $2 \times 2\mu\text{m}^2$  transistor are also marked. The overlapping between coarse curves allows fine resolution no matter what desired current is chosen, which would not be true for a non-overlapping case. All eight fine tuning curves are approximately linear with the fine selection codes. However, according to simulation, the minimum  $I_{\text{INF}}$  achievable at higher temperature is substantially larger mainly due to the junction leakage currents contributed by switches in R-2R current divider, about several pA at 80°C, which limits the precision and also the practical DR to only about 130dB [10].

## 5. DISCUSSION

Table 2 summarizes the specifications. The area of each bias is about 25% of the previous design [3] thanks to removal of SRs. The measured dynamic range is extended to over 170dB with less configuration bits due to the coarse-fine architecture. The power consumption of

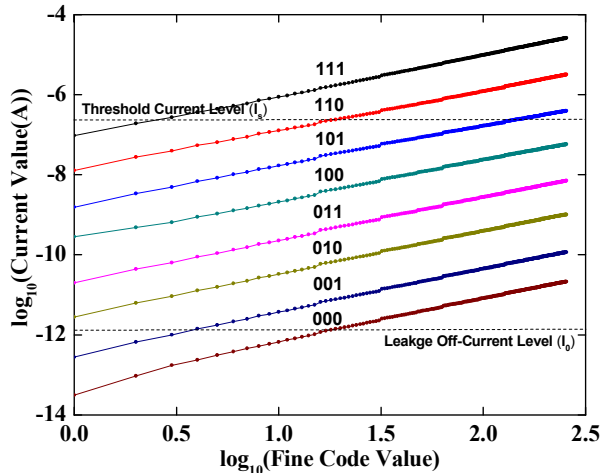


Fig. 7 Measured current tuning curves at room temperature.

each bias is scaled according to the selected coarse current and the biasing voltage type in the buffer, instead of being a fixed up-scaling of the master current. Preliminary measurements also show less than  $\pm 10\%$  ( $1-\sigma$ ) mismatch between all biases over all ranges within one chip. DNL is found to be larger than -1, which means no non-monotonicity. The worst DNL is around 5LSB that happens at the transition of fine bits from 01111111 to 10000000. This suggests that nonlinearities could be reduced by regulating the voltage at the output node of the R-2R current divider at the cost of increased silicon area. The on-chip calibration circuit is also functional for currents larger than about 100pA.

**Table 2.** Specifications of current reference array.

Technology	180nm 1P6M CMOS
Supply voltage	1.8V
Master current area	375 $\mu\text{m} \times 125\mu\text{m}$
Single Bias area	360 $\mu\text{m} \times 22\mu\text{m}$
Bias dynamic range	>170dB (at 25°C)
Current consumption per bias	$\sim 2I_{Ci}$ ( $i=1\sim 7$ ) N-type $\sim 3I_{Ci}$ ( $i=1\sim 7$ ) P-type

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