Latchup: What it is and how to avoid it. (For neophytes)

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Latchup is a problem that sometimes occurs when either a design rule is violated or there was a problem with the process. The result is that when you power up your chip everything looks ok until you get to a certain supply voltage, and then **WHAMMO**, the chip looks like it's shorted to ground. The problem arises from intrinsic bipolar structures in the CMOS process that can amplify each other's current. What this document is intended to do is explain how this can come about and what the one can do to avoid the problem.

1 What latchup is

The way to understand latchup is from combining a knowledge of how bipolar (i.e. *pnp* and *npn*) transistors work in a circuit with a knowledge of the CMOS layering scheme. The first figure shows a generic CMOS structure in vertical cross section. There are a number of *p* and *n* regions formed by the substrate, the well, and the diffused regions. One possible circuit that incorporates the two bipolar transistors (one *pnp* and the other *npn*) that are evident in Fig. 1 is shown in Fig. 2. A little thought will show what this circuit implies. The figure captions explain further.

2 How to avoid it

The fix to all this is extremely simple. First, obey the design rules; this keeps R1/R2 and R3/R4 small. Second, make sure to tie all the wells to the supply voltage and ground the substrate liberally. This is equivalent to tying the base of Q1 to Vdd and the base of Q2 to ground. The relevant design rules are

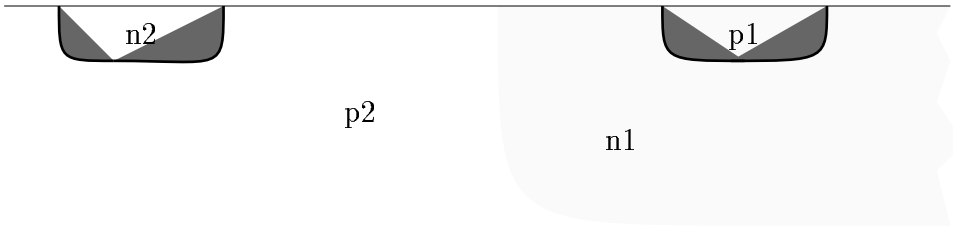

Figure 1: The vertical structure of an n-well CMOS design. The well is the large diffused n-type region, while the other diffused regions are active regions that make up the transitors. The labeling corresponds to the labeling in Fig. 2. If the well is not kept near enough to the supply voltage the junction between the n-well and the p-type active in the well becomes forward biased. Then we have a forward biased *pnp* transistor. Similarly, if the p-type substrate is not kept well grounded, the junction between some n-type active in the substrate and the p-type substrate can become forward biased (remember the voltages are opposite) and we can have an *npn* bipolar transistor. In the first case the collector is the substrate, while in this case the well serves as the collector.

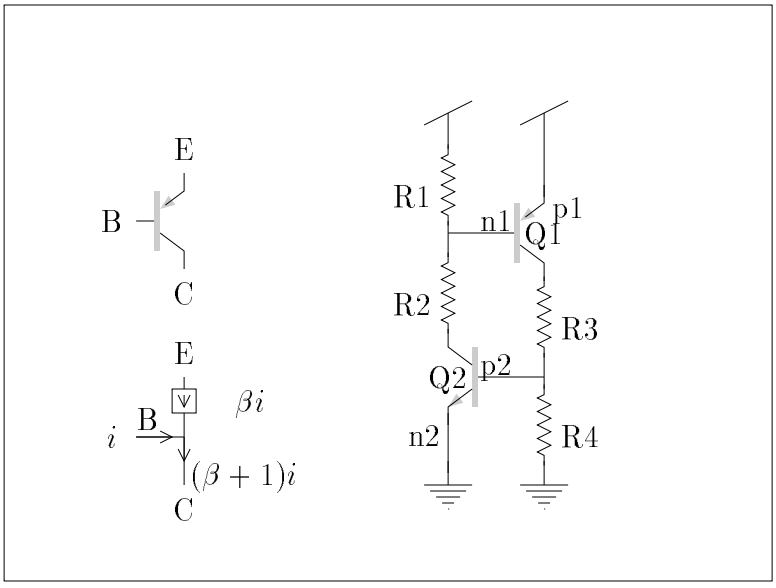

Figure 2: A possible circuit arising from Fig. 1. The conventions for bipolar transistor symbols are shown on the left, where E stands for emitter, B for base, and C for collector. The most important points about transistors: the base current is amplified by β, and the base current is exponential in the base-emitter voltage V_{BE}. Below the symbol is the usual first cut for a model of this transistor. If R1/R2 is not kept small then Q1 can become turned on. That will result in some current which can feed into the base of Q2 (if R3/R4 is not small), which results in feedback to the base of Q1, and so on. The result is latchup. Both Q1 and Q2 are on as much as they can be.

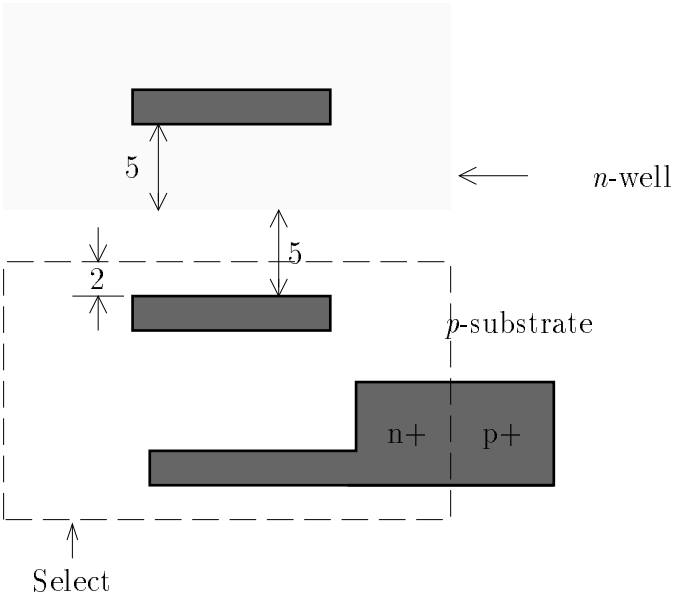

Figure 3: The relevant design rules and a diode formed by an improper substrate contact. The substrate is p-type. The active inside the select is n+, while the substrate contact is p+. Thus we have a n+/p+ diode sitting on a p substrate. Ordinarily the substrate will be near ground potential, while the n+ active will be at some higher potential. The p's will be pulled towards ground and the n's towards Vdd; thus, the diode will be reverse biased. If the voltage exceeds a nominal 3V, however, the diode will break down. In other words, you will be Zenered to death.

shown in Fig. 3. Keeping green stuff 5λ inside the well and 5λ away from the well is enough space so that R1/R2, R3/R4, and the various β's are small enough to prevent latchup.

3 Appendix: A problem which may appear to be latchup but isn't

In the current set of design rules one can make a substrate contact by extending some active out of a selected region, and then making sure that a contact to this active is at least 2λ away from the select region. This is shown in Fig. 3. This forms a diode at the edge of the select region. This would ordinarily appear to be ok, since the diode would be reverse biased. But it so happens that because these diodes are heavily doped, they have a reverse breakdown voltage of about 3 volts. So suddenly at 3 volts these diodes will start conducting heavily to the substrate, and it will appear to you that you have shorted Vdd to ground. The fix: make sure the diode is shorted by some metal.