ETH Course 402-0248-00L: Electronics for Physicists II (Digital)

- 1: Setup uC tools, introduction
- 2: Solder SMD AVR32 board
- 3: Build application around AVR32 finish today
- 4: Design your own PCB schematic
- 5: Place and route your PCB
- 6: Start logic design with FPGAs

Exercise 3: "Sound volume robot"

- measures sound volume and moves arm to indicate loudness
- microphone -> preamp -> ADC -> uC -> PWM output



"RC" servos (Radio-Control Servo-Motors)



- Pulse width from 1-2ms sets desired position
- Pulses must be sent at frequency 50-200Hz Pulse height >2V

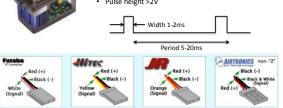
Microphone + Preamp

1/4 LM324

56k

328k

Vdd Servi



3.31

33

N4W7

D

10000 MF ilv

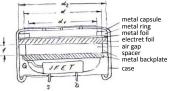
え

mic

VBUS 15

Electret Microphone

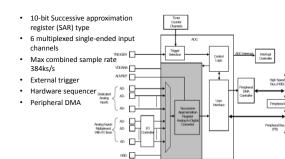
- Cheap (< 1\$) .
- Electret material, no polarization voltage is required
- Low-noise JFET buffer
- Metal foil is connected to source of the JFET through metal capsule







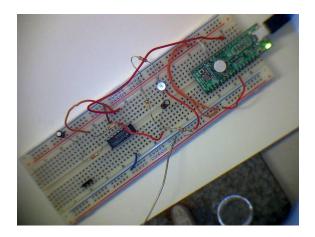
AVR32 Analog to Digital converter



Ik Servo power supply

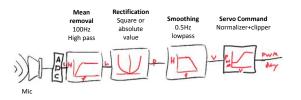
Vand

100k



- Fixed-point digital signal processing pipeline
- Using timer interrupts for regular ADC sampling intervals

Signal processing pipeline produces servo position corresponding to average sound volume

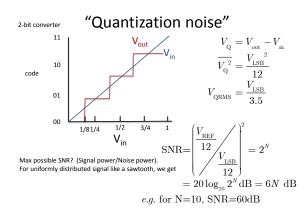


Some more about ADCs

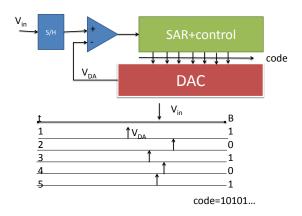
High resolution Low speed and power	Medium resolution Medium power	Low resolution but fast and hot
Single slope (imprecise)	SAR (good tradeoffs, most uC)	Flash (video rate, oscilloscopes)
Dual slope (precise but very slow)	Algorithmic ($\Sigma\Delta$)	2-step

ADC specifications

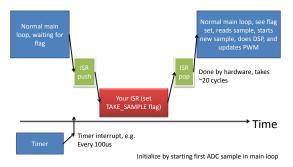
INL	Integral nonlinearity	Max absolute sample deviation in bits
DNL	Differential nonlinearity	Max possible step size variation in bits
Sample rate		
Latency	In samples	How long in samples it takes for a conversion (can be >>1 for pipelined converter)
Reference voltage	Volts	Minimum resolution



Successive Approximate Register (SAR) ADC SAR+control code $V_{\underline{DA}}$ DAC



Using timer interrupts for regular ADC sampling intervals in an Interrupt Service Routine (ISR)



ISR

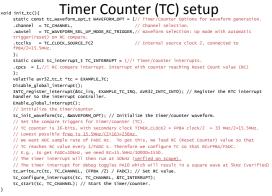
static void tc_irq(void) { // Increment the counter, which is also used to
determine servo updates tc_tick++;

// set a flag to tell main loop to take a sample takeSampleNow = TRUE;

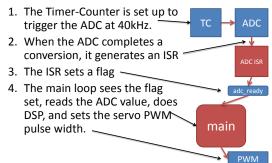
// Clear the interrupt flag. This is a side effect
of reading the TC SR.
tc_read_sr(EXAMPLE_TC, TC_CHANNEL);

// Toggle a GPIO pin (this pin is used as a regular GPIO pin). gpio_local_tgl_gpio_pin(AVR32_PIN_PA10); // debug, should toggle at desired sample rate

}



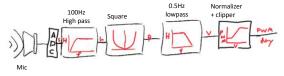
Alex Hungenberg tried the following hardware-driven approach



What's wrong with this ISR? _attribute__((__interrupt__)) static void adc_int_handler(void) { adc_ready = 1; volatile avr32_adc_t *adc = &AVR32_ADC; update_pwm(*((unsigned long *)(&(adc->cdr0)))); ADC End Of 25.7.6 Status Register status EOC2 Conversion SR register Name: bit EOCn: End of Conversion n These bits are set when the corresponding conversion is complete These bits are cleared when the corresponding CDR or LCDR registers are read. 0: Corresponding analog channel (if implemented) is disabled, or the conversion is not finished. 1: Corresponding analog channel (if implemented) is enabled and conversion is complete

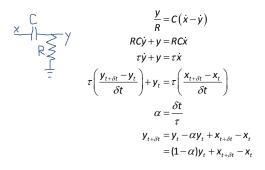
- 1. The ISR is triggered by the ADC.
- 2. Because Channel Data Register is not read in the ISR, the interrupt flag is not cleared.
- 3. The interrupt is immediately re-triggered, so the main loop always sees the flag set.

Fixed point signal processing pipeline



We need a digital low & high pass filters, like an RC or CR filter

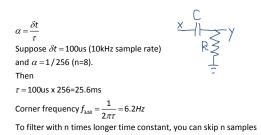
A simple IIR high pass filter (discrete time)



A simple IIR high pass digital filter (fixed point, using binary shift operations)

$$\begin{array}{c} X \\ \hline \\ R \\ \hline \\$$

What is the time constant?



DSP code sample

```
void device_task(void) {
```

}

```
if (takeSampleNow) { // flag set in timer ISR
gpio_local_tgl_gpio_pin(AVR32_PIN_PA11); // debug
takeSampleNow=FALSE;
// signal processing
S16 adcval = (S16)get_adc_value(); // 0-1023=3.3V
if (initialized)
          audMean = ((adcval-audMean)>>NTAU1)+audMean; // TODO mix old and new value
else
          audMean = adcval; // init filter with first reading
// only update meanSq at TAU2 interval, so to produce effective time constant that is TAU2 times tau of audwean filtering if(dspcounter-===0)(
    dspCounter=TAU2;
long diff = adcval - audMean; // signed <u>diff of sample from mean</u>
    long sq = diff * diff; // square diff
if (initialized)
          meanSq = ((sq-meanSq)>>NTAU1)+meanSq; // low pass square diff
     else
          meanSq = sq;
```

USB – Universal Serial Bus

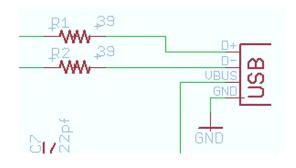
- Physical layer
- User perspective (coder)
- · Under the hood
 - Device side
 - Host side
- · Achieving high performance

USB Physical layer Up to 200mA 0.2 +5V • Up to USB 2.0 - full (12Mbps) and high (480Mbps) speed • USB 3.0 super speed Ground Data-Low voltage (5Ggbs) differential signal Transmit + Receive -Transmit -Receive + Ground

USB definitions

- IN means towards the host (the PC)
- OUT means towards the device (uC)

USB on PCB



USB user perspective (as coder) Device side - Include USB driver

#include "usb_task.h"

#if USB_DEVICE_FEATURE == ENABLED
#include "usb_derv.h"
#include "usb_descriptors.h"
#include "usb_standard_request.h"
#include "device_task.h"
#endif

static U8 in_buf[EP_SIZE_TEMP1]; static U8 out_data_length; static U8 out_buf[EP_SIZE_TEMP2]; //!
//! @brief This function initializes

static U32 sof_cnt;

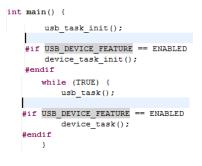
static U8 in_data_length;

//!
void device_task_init(void) {
 sof_ont = 0;
 in_data_length = 0;
 out_data_length = 0;

Usb enable sof interrupt(); //! This function increments the sof_cnt counter each time //! The USB Start-of-Frame interrupt subroutine is executed (1 mg). //! Useful to manage time delays

//!
void usb_sof_action(void) {
 gpio_local_tgl_gpio_pin(AVR32_PIN_FA10);
 sof_ont++;

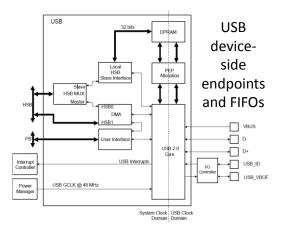
Main loop



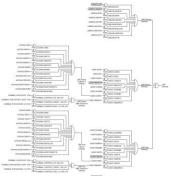
Usb_reset_endpoint_fifo_access(EP_TEMP_IN); usb_write_ep_txpacket(EP_TEMP_IN, in_buf, in_data_length, NULL); in_data_length = 0; Usb_ack_in_ready_send(EP_TEMP_IN);

OUT direction

// If we receive something in the OUT endpoint,
// Just store it in the RAM buffer
if (Is_usb_out_received(EP_TEMP_OUT)) {
 gpio_local_tgl_gpio_pin(XVR32_PIN_PA12);
 Usb_reset_endpoint_fifo_access(EP_TEMP_OUT);
 out_data_length = Usb_byte_count(EP_TEMP_OUT);
 usb_read_ep_rxpacket(EP_TEMP_OUT, out_buf, out_data_length, NULL);
 Usb_ack_out_received_free(EP_TEMP_OUT);
 // update FWM:
 set_rgb(out_buf[1], out_buf[2], out_buf[3]);



USB interrupts (you don't worry about them!)

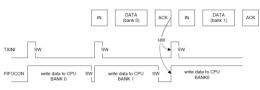


Endpoints - multiple virtual channels

Pipe/Endpoint	Mnemonic	Max. Size	Max. Nb. Banks		DMA	Type Control		
0	PEP0	64 bytes			N			
1	PEP1	64 bytes		2		Y	Isochronous/Bulk/Interr	
2	PEP2	64 bytes		2		Y	Isochronous/Bulk/Interr	
3	PEP3	64 bytes		2		Y	Isochronous/Bulk/Interr	
4	PEP4	64 bytes		2		Y	lsochronous/Bulk/Interr	
5	PEP5	256 bytes		2		Y	Isochronous/Bulk/Interr	
6	PEP6	256 bytes		2		Y	Isochronous/Bulk/Interr	

Can be double buffered

Double-buffered transfers can increase continuity



When the bank is empty, TXINI and FIFOCON are set, what triggers an EPnINT interrupt if TXINE is one.

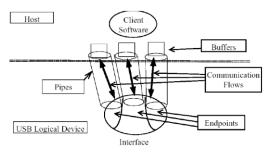
The user acknowledges the interrupt by clearing TXINI.

 The user writes the data into the current bank by using the USB Pipe/Endpoint nFIFO Data virtual segment (see "USB Pipe/Endpoint n FIFO Data Register (USBFIFOnDATA)" on page 483), until all the data frame is written or the bank is full (in which case RWALL is cleared and the Byte Count (BYCT) field in UESTAn reaches the endpoint size).

The user allows the controller to send the bank and switches to the next bank (if any) by clearing FIFOCON.

Host vs. Device

For the USBB in host mode, the term "pipe" is used instead of "endpoint" (used in device mode). A host pipe corresponds to a device endpoint





/def main(): dev = get_device() try: dh = dev.open() dh.claimInterface(IFACE) rainbow(dh) dh.releaseInterface() del dh return 0 except : print "no avr32 found?", sys.exc_info()

The key to high performance on host side: Asynchronous or Overlapped IO

- On the host side, an Input-Output (IO) thread manages the USB IO.
- Multiple buffers (which can be much larger than the device FIFO size) are submitted to the USB driver / host controller to be filled by the USB controller.
- 1. When a buffer is filled, the IO thread is notified asynchronously, which wakes it up.
- The IO thread processes the buffer, and then gives it back to the controller. The IO thread then notifies the main user code that data is available, e.g. by writing to a software queue.
- · That way, the user doesn't block waiting for data
- Our *pyusb* example doesn't do this yet

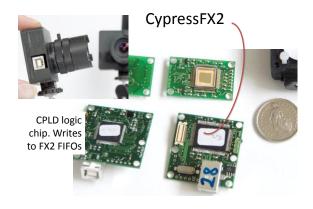
ubblocht = 0L Bdef ubblo(dp, r, g, b): global ubblocht ubblocht + 1 dout = array.array('B', [0]*4) dout[0] = 0xFF & 0x00 dout[1] = 0xFF & (r) dout[2] = 0xFF & (r) dout[2] = 0xFF & (r) dout[3] = 0xFF & (b) dh.bulkWrite(EP_OUT, dout.tostring()) #if ubblocht % PWMperADC == 0: if 1: din = dh.bulkRead(EP_IN, 4) l = len(din) if 1 != 4: print "unexpected bulk read length: %d" % 1 else: if ubblocht % PWMperADC == 0: add((din[2] << 8) + din[3])</pre>

USB performance

- USB full speed (12Mbps): about 1MBps
- USB high speed (480Mbps): about 40MBps
- USB super speed (5Gbps): ??

ICs for USB

USB full speed	• Many uC. Also FTDI.
USB high speed	• CypressFX2
USB super speed	• CypressFX3







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Cypress EZ-USB \otimes FX3^m is the next-generation SuperSpeed USB 3.0 peripheral controller that enables developers to add USB 3.0 device functionality to any system.

EZ-USB FX3 has a fully configurable, General Programmable Interface (GPIF[™] II) that can interface with any processor, ASIC, image sensor, or FPGA. GPIF[™] II is an enhanced version of the original GPIF[™] in FX2LP, Cypress's flagship USB 2.0 product. It provides easy and glue-less connectivity to popular industry interfaces such as

ftdichip.com

- uC UART USB interface; looks like COM serial port on host side.
- Max speed is only 12Mbaud for the UART port unfortunately

USB IN THE FAST LANE

