Bias Current Generator

Patrick Lichtsteiner

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Institute of Neuroinformatics, University/ETH Zürich, 8057 Zürich

Contents

Introduction

This report presents an analysis of instability in a bias current generator. It is divided up in six chapters. The first chapter presents the circuit. It is followed by the discussion of a measurement which exposes that the circuit turns out to be unstable under certain conditions. The next three chapters offer a mathematical approach to find stability criteria. The thesis is closed with conclusions and with propositions to improve the stability of the circuit.

1. Masterbias

A bias current generator (hereafter called masterbias) provides a known, steady current directly on chip. This current can afterwards be multiplied, divided or converted into voltages. This technique grants a good handling of the device even by inexperienced users and makes more pins available for outputs inputs.
As a lot of circuits are highly sensitive to changes in current or voltages, a masterbias has to be very stable.
The masterbias presented in figure 1.1 is used on the chip friend 10, physiology helper, based on a CMOS version of Widlor's bootstrapped bias circuit. The masterbias consists of a start up mechanism (shown in green), two transistors that allow enabling or disabling the masterbias, a p-fet mirror and a cascaded n-fet mirror. The start up mechanism is needed to ensure that the mirrors are not stuck in a steady state which inhibits its proper use. This could happen if the circuit starts up at zero current which is a stable operating point. In this case, the start up mechanism pushes some current into the right side and gets the circuit going.
The n-fet mirror is cascaded to reduce the Early effect of supply voltage variations. The n-fet transistor marked with the M has a W/L ratio which is M times larger then its left neighbours. The nbias node provides the voltage to duplicate th current. The nodes Vres and Rx are brought out to pins. The access to this nodes allows to change the current through the masterbias and provide access for measurements. With Vres, the resistor on chipcan be exchanged with a resistor of a

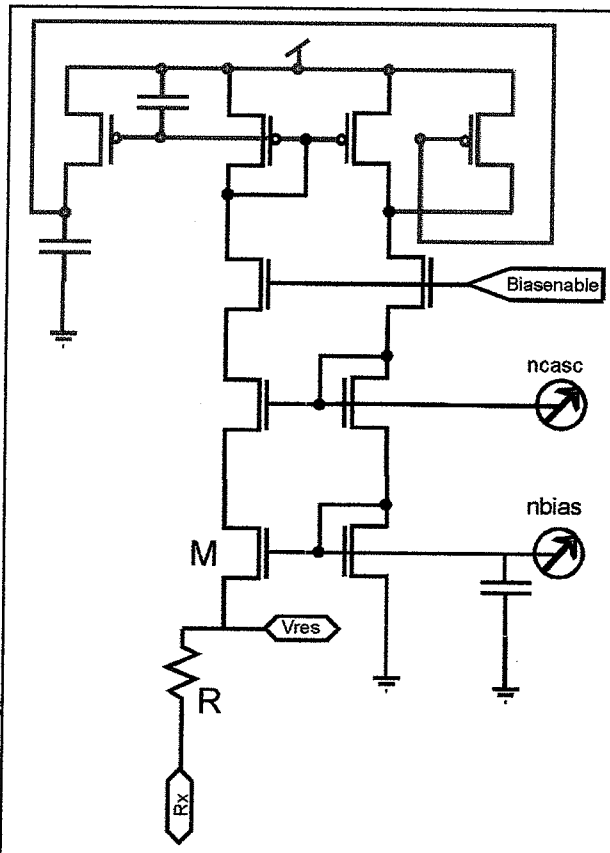

Figure 1.1: Bias current generator. In green colour is the start up mechanism visible. The node nbias is used as output. Rx, Vres and Biasenable are brought out to pins.

different value outside of the chip. The current through the transistor above the resistor R is exponentially dependent on its source voltage. The source voltage is via Ohm's law related to the resistor and can therefore be influenced by the resistance. The voltage above the n-fet M changes so that the currents through both sides of the circuit are the same and the materbias reaches a stable point of operation. This allows to set the current to a desired value.
With largely different values of R the modes of operation of the circuit can be changed from weak inversion to strong inversion. In the subthreshold model, the currents through the n-fet transistors in saturation are given by the following equations:

$$I_1 = MI_0 e^{\kappa V_g / U_T - V_s / U_T} = MI_0 e^{\kappa V_g / U_T - I_1 R / U_T} \tag{1.1}$$

$$I_2 = I_0 e^{\kappa V_g / U_T} \tag{1.2}$$

where I_1 is the current through the left transistor, V_g is the gate voltage of the n-fet mirror and V_s is the source voltage of the left transistor. In steady state, the two currents are equal:

$$I_2 = I_1 \equiv I \tag{1.3}$$

$$MI_0 e^{\kappa V_g / U_T} = MI_0 e^{\kappa V_g / U_T - I_1 R / U_T} \tag{1.4}$$

This provides a simple equation for the current I and the source voltage in the subthreshold region:

$$I = \frac{1}{R} U_T \ln(M) \tag{1.5}$$

$$V_s = U_T \ln(M) \tag{1.6}$$

If the resistor R is smaller than 50Kohm the current gets large enough that the strong inversion model is more adequate for calculations. In the above threshold saturation region the currents through the transistors can be written as:

$$I_1 = M \frac{\beta}{2} (V_g - V_T - V_s)^2 = M \frac{\beta}{2} (V_g - V_T - I_1 R)^2 \tag{1.7}$$

$$I_2 = \frac{\beta}{2} (V_g - V_T)^2 \tag{1.8}$$

Where V_T is the threshold voltage. In the steady state the currents are equal. This leads via (1.3) to the following equations:

$$M \frac{\beta}{2} (V_g - V_T - IR)^2 = \frac{\beta}{2} (V_g - V_T)^2 \tag{1.9}$$

$$I = \frac{\left(1 - \sqrt{M}\right)(V_T - V_g)}{\sqrt{M} R} \tag{1.10}$$

The gate source voltage V_{gs} of M is about V_T whereas V_{gs} of the right n-fet is then the sum of the threshold voltage and IR. This assumption is grounded on the large ratio of W/L of M. This leads to a simple equation for I:

$$I = \frac{2L}{\beta W R^2} \tag{1.12}$$

This calculations show that the models predict that the current is proportional to 1/R below threshold and to $1/R^2$ above threshold.
Figure 1.2 shows the current I as a function of the resistor R in a log-log plot for the measurement, a Tspice simulation and the two models. The Tspice simulation matches the measurements pretty well. In strong inversion, the model turns out to be inadequate.

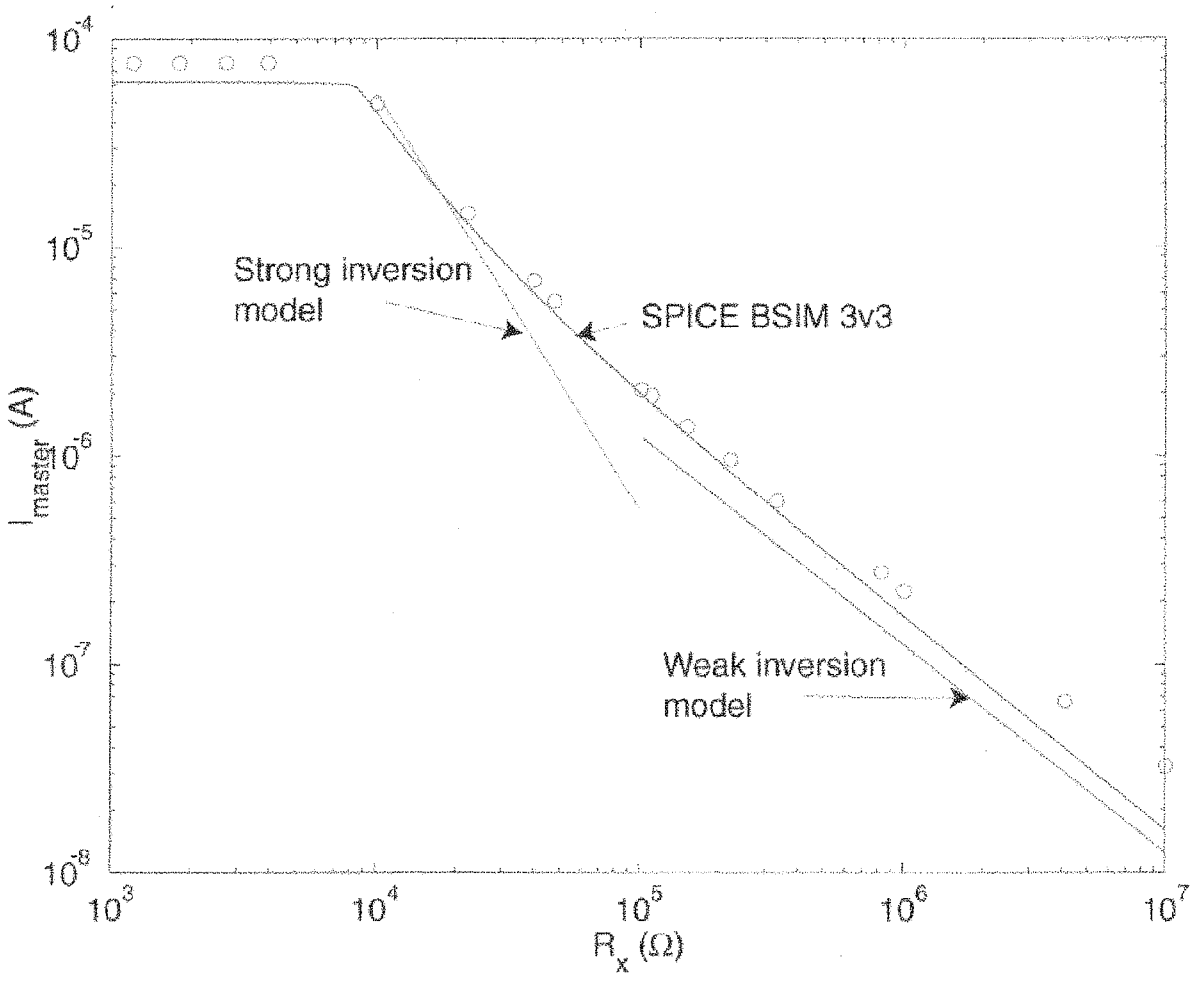

Figure 1.2: Mastercurrent I as a function of the resistor R. The red dots display the measurements. The blue line is the output of a tspice simulation. The subthreshold and the above threshold model are printed in green. To reduce the capacitance on Vres and therefore to improve the stability of the circuit, single resistors were used on pin Vres.

The subthreshold equations for M_1 and M_2 are:

$$I_1 = MI_0 e^{\kappa V_g / U_T - V_s / U_T} \tag{3.1}$$

$$I_2 = I_0 e^{\kappa V_g / U_T} \tag{3.2}$$

The total change in the current, i_1 and i_2, due to small variations in V_g, V_d and V_s (referenced to the bulk, V_b) can be described as follows:

$$i_1 = g_{m_1} \Delta V_g - g_s \Delta V_s \tag{3.4}$$

$$i_2 = g_{m_2} \Delta V_g \tag{3.5}$$

where

$$g_{m_1} = \frac{dI_1}{dV_g} = \frac{\kappa I_1}{U_T} \tag{3.6}$$

and

$$g_{m_2} = \frac{dI_2}{dV_g} = \frac{\kappa I_2}{U_T} \tag{3.7}$$

are the transconductance of M_1 and M_2 respectively and

$$g_s = -\frac{dI_1}{dV_s} = \frac{I_1}{U_T} \tag{3.8}$$

is the source conductance of M_1. The source conductance of M_2 does not matter because the source is directly hooked to ground. The drain conductance of M_1 and M_2 can be neglected because the two n-fets are in saturation.
The difference of i_1 and i_2 charges up the gate capacitance C_g, because I_1 has to equal I_2:

$$i_1 - i_2 = C_g \frac{dV_g}{dt} \tag{3.9}$$

and with equations (3.4) and (3.5) this leads to:

$$C_g \frac{dV_g}{dt} = (g_{m_1} - g_{m_2}) \Delta V_g - g_s \Delta V_s = -g_s \Delta V_s \tag{3.10}$$

A corresponding equation can be found for the drain capacitance of M_1:

$$C_S \frac{dV_s}{dt} = g_{m_1} \Delta V_g - g_s \Delta V_s - \frac{\Delta V_s}{R} \tag{3.11}$$

Assume:

$$\Delta V_g \equiv v_g e^{ts} \ , \ \Delta V_s \equiv v_s e^{ts} \tag{3.12}$$

The equations (3.10) and (3.11) change into:

$$C_g s\Delta V_g = -\frac{I}{U_T}\Delta V_s \tag{3.13}$$

$$C_s s\Delta V_s = \frac{\kappa I}{U_T}\Delta V_g - \frac{I}{U_T}\Delta V_s - \frac{\Delta V_s}{R} \tag{3.14}$$

The following constants simplify (3.13) and (3.14)

$$\tau_g \equiv \frac{C_g U_T}{I}, \quad \tau_s \equiv \frac{C_s}{\frac{I}{U_T}+\frac{1}{R}}, \quad \alpha \equiv \frac{I\kappa}{I+\frac{U_T}{R}} \tag{3.15}$$

to

$$\Delta V_s = -\tau_g s\Delta V_g \tag{3.16}$$

$$\Delta V_s(\tau_s s+1) = \alpha\Delta V_g \tag{3.17}$$

A quadratic equation for s is obtained by replacing ΔV_s in (3.17) with (3.16). The solution

$$s_{1,2} = \frac{-\tau_g \pm \sqrt{\tau_g^{\,2} - 4\tau_g\tau_s\alpha}}{2\tau_g\tau_s} = \frac{-1 \pm \sqrt{1-4\frac{\tau_s}{\tau_g}\alpha}}{2\tau_s} \tag{3.18}$$

provides a stability criteria for the differential equations (3.10) and (3.11)

$$\boxed{4\frac{\tau_s}{\tau_g}\alpha \le 1 \quad \Rightarrow \quad C_s \le \frac{C_g}{4\kappa}\left(1+\frac{U_T}{IR}\right)^2} \tag{3.19}$$

This result predicts that the stability of the circuit depends on the ratio of the source capacitance and the gate capacitance. In the subthreshold saturation mode of operation a ratio of ten ensures a small signal stability of the used circuit. This ratio and also the ones proposed by further calculations could not be verified experimentally because the capacitance of the gate of the n-fet mirror on the chip friend 10 can not be influenced from the outside.

4. Differential equations for two capacitances

The small signal calculations are adequate only for small variations in the terminals of the transistors and low frequencies. In the same model (figure 3.1) a set of two differential equations can be obtained directly for large signal.

Using (3.1) and (3.2), the current flowing into C_g and C_s can be written as:

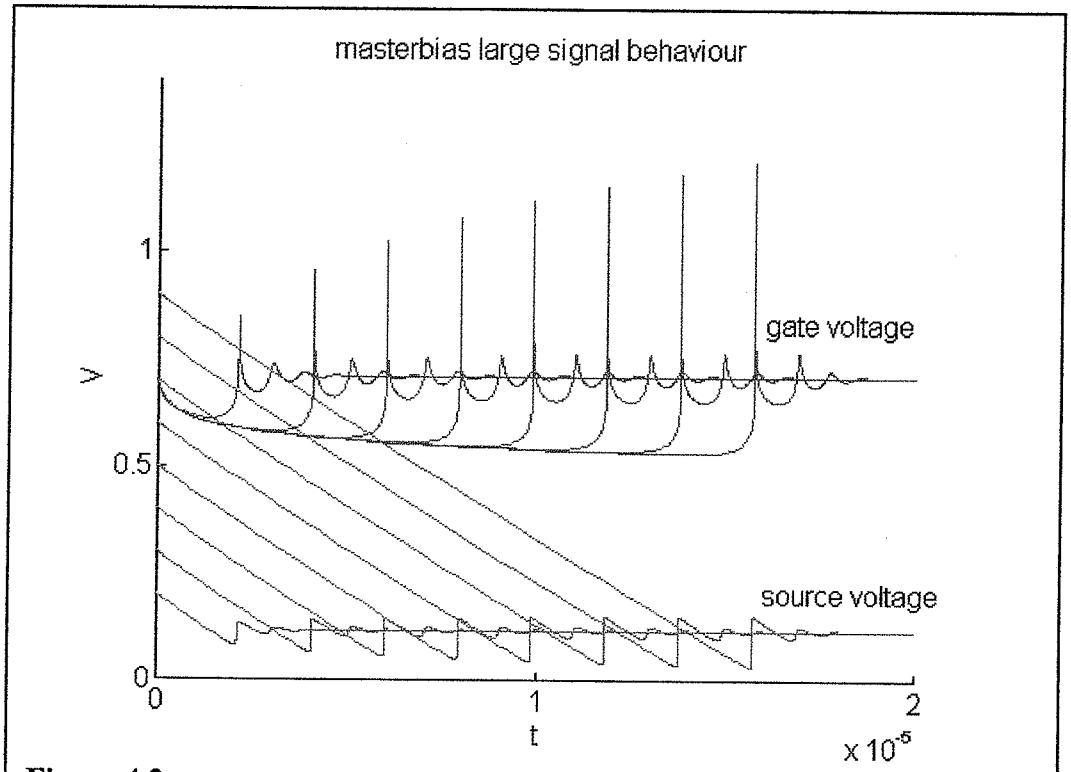

Figure 4.2: Gate and source voltage as a function of time for different starting values of the source voltage. The source capacitance C_s=1e-10 and the gate capacitance C_g=2e-12.

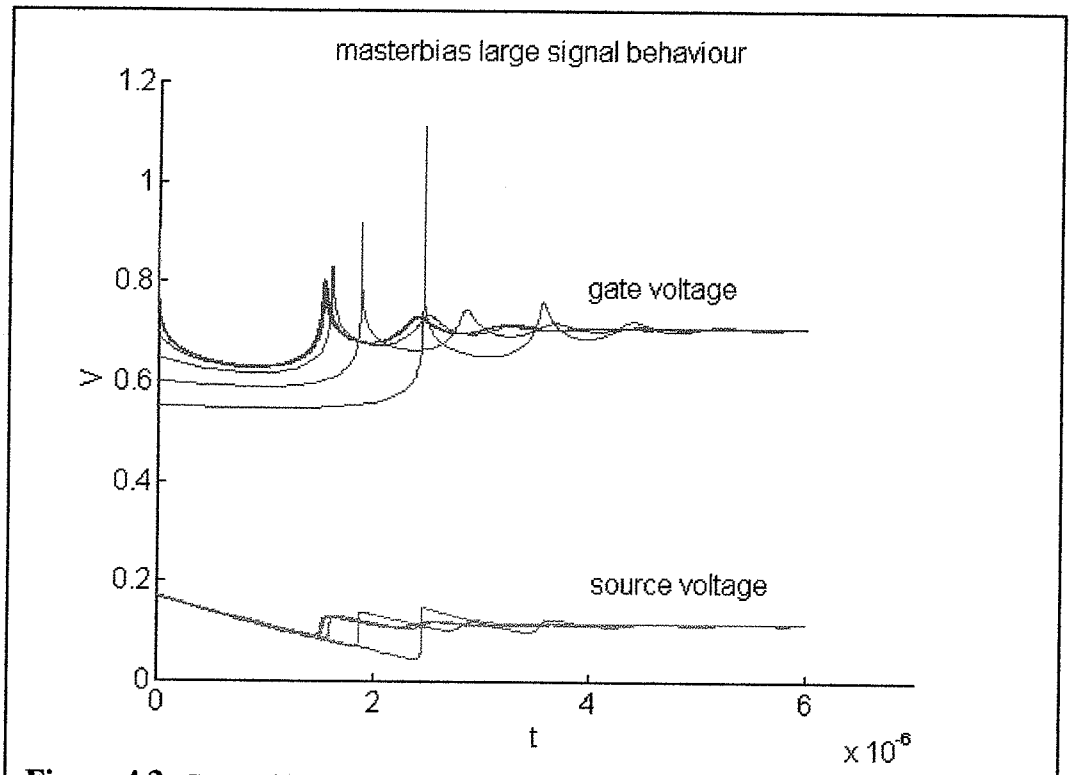

Figure 4.3: Gate and source voltage as a function of time for different starting values of the gate voltage. The source capacitance C_s=1e-10 and the gate capacitance C_g=2e-12.

5. Differential equations for three capacitances

Instead of assuming a perfectly fast mirror, the p-fet mirror can be taken into account in a broadened model, which consists of three capacitances. The additional capacitance Cm models the gate capacitance of the p-fet mirror and so also its time delay. The schematic is shown in figure 5.1. To create the differential equations, three currents are needed. The following calculation assumes subthreshold conditions with all transistors in saturation. The currents through the n-fet transistors are given by (3.1) and (3.2). The p-fet transistors are of the same dimensions and their source is linked to Vdd. Therefore the current through both of them is the same and can be calculated (in subthreshold and saturation) as follows:

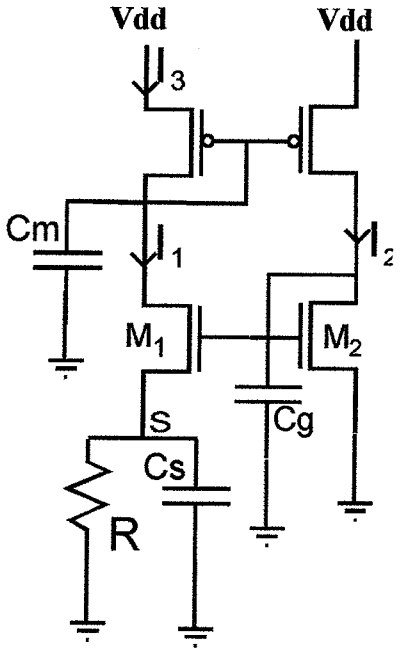

Figure 5.1: masterbias circuit with three capacitances

$$I_3 = I_{p0} e^{\kappa (V_{Vdd} - Vm)/U_T} \tag{5.1}$$

The differential equations are formed, as in the previous part, by writing the current flowing into a capacitance as the difference of the currents flowing through the transistors and the resistor:

$$C_m \frac{dV_m}{dt} = I_3 - I_1 = I_{p0} e^{\kappa (V_{Vdd} - Vm)/U_T} - MI_0 e^{\kappa Vg/U_T - Vs/U_T} \tag{5.2}$$

$$C_g \frac{dV_g}{dt} = I_3 - I_2 = I_{p0} e^{\kappa (V_{Vdd} - Vm)/U_T} - I_0 e^{\kappa Vg/U_T} \tag{5.3}$$

$$C_S \frac{dV_s}{dt} = I_1 - \frac{V_s}{R} = MI_0 e^{\kappa Vg/U_T - Vs/U_T} - \frac{V_s}{R} \tag{5.4}$$

As before a non-linear system of differential equations is acquired by solving (5.2) to (5.4) for the derivatives of the gate voltage of the p-fet transistors V_m, the gate voltage of the n-fet transistors V_g and the source voltage of M_1:

$$\frac{dV_m}{dt} = \frac{1}{C_m}\left(I_{p0} e^{\kappa (V_{Vdd} - Vm)/U_T} - MI_0 e^{\kappa Vg/U_T - Vs/U_T}\right) \tag{5.5}$$

$$\frac{dV_g}{dt} = \frac{1}{C_g}\left(I_{p0} e^{\kappa (V_{Vdd} - Vm)/U_T} - I_0 e^{\kappa Vg/U_T}\right) \tag{5.6}$$

$$\frac{dV_s}{dt} = \frac{MI_0}{C_s} e^{\kappa Vg/U_T - Vs/U_T} - \frac{V_s}{C_s R} \tag{5.7}$$

This differential equations can be solved numerically. A time step model predicts a critically damped behaviour for a ratio C_g:C_s of about 1 with a ratio C_g:C_m of 1e3. The output for the values I_o=1e-15[A], κ=0.8, U_t=0.025[V], M=100, R=1e5[Ω],C_m=1e-14[F], C_s=1e-11[F] and C_g=1e-13, 5e-12, 1e-12[F] is illustrated in figure 5.2

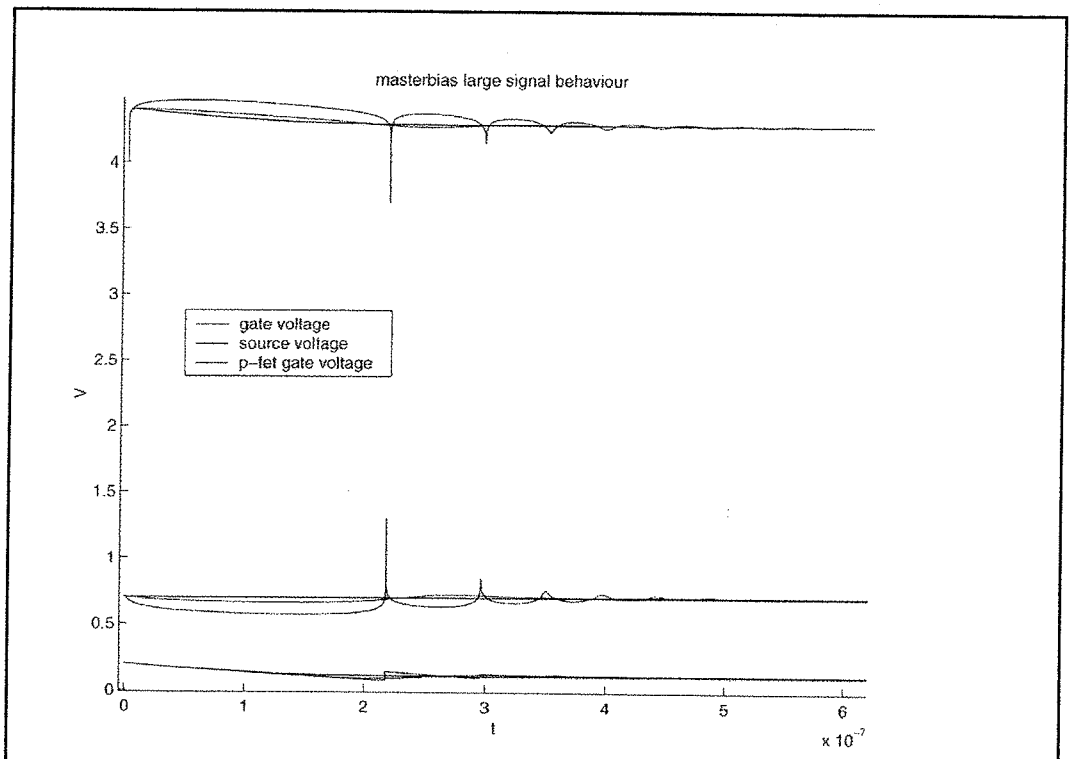

Figure 5.2: N-fet gate, p-fet gate and source voltage as a function of time. The source capacitance C_s=1e-10, the p-fet gate capacitance C_m=1e-13 and the gate capacitance C_g=2e-12, 1e-11. 1e-10.

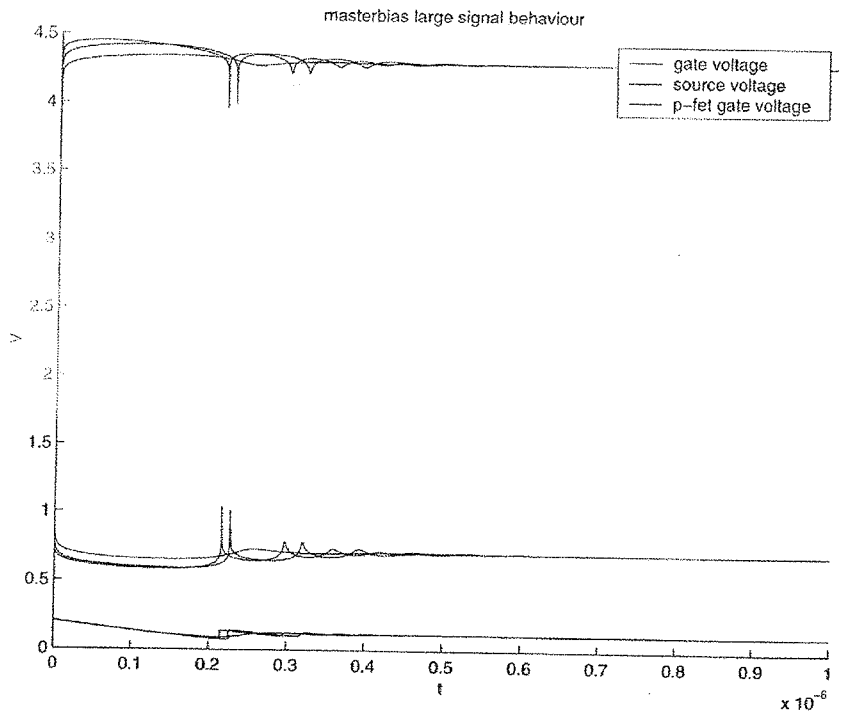

Figure 5.3: N-fet gate voltage V_g, p-fet gate voltage V_m and source voltage V_s as a function of time. The source capacitance C_s=1e-10, the gate capacitance C_g=2e-12 and the p-fet gate capacitance Cm=1e-14, 1e-12, 1e-11.

The amount of the p-fet gate capacitance C_m largely affects the stability of the circuit. The larger the p-fet capacitance is, the more the oscillation is damped and the more stable the circuit gets. A printout for three different values of C_m is shown in figure 5.3.

6. Conclusions and propositions

All the calculations in section 3 to 5 and also simulations with Analog and Tspice suggest that the stability of the masterbias circuit depends on the ratio of C_g:C_s. Furthermore, the circuit should be stable for a ratio of C_g:C_s higher then 10. Unfortunately the capacitance of the gate of friend 10 can not be raised from the outside due to a transconductance amplifier between the gate and the pin. This means that the stability of the circuit can not be improved by adding capacitances and the mathematical models and the simulations can not be verified by measurements.

The numerical integrations of the differential equations for the three capacitance model and also the Analog simulations, see figure 5.3 and figure 2.3, show that the gate voltage of the p-fet mirror and the gate voltage of the n-fet mirror oscillate in opposite directions and that the oscillation also depends on the value of the gate capacitance of the p-fet mirror. This also shows that the mirror is fast and the calculations in section 4 are adequate.
As visible in figure 5.3, a larger capacitance on the p-fet gate damps the oscillation.

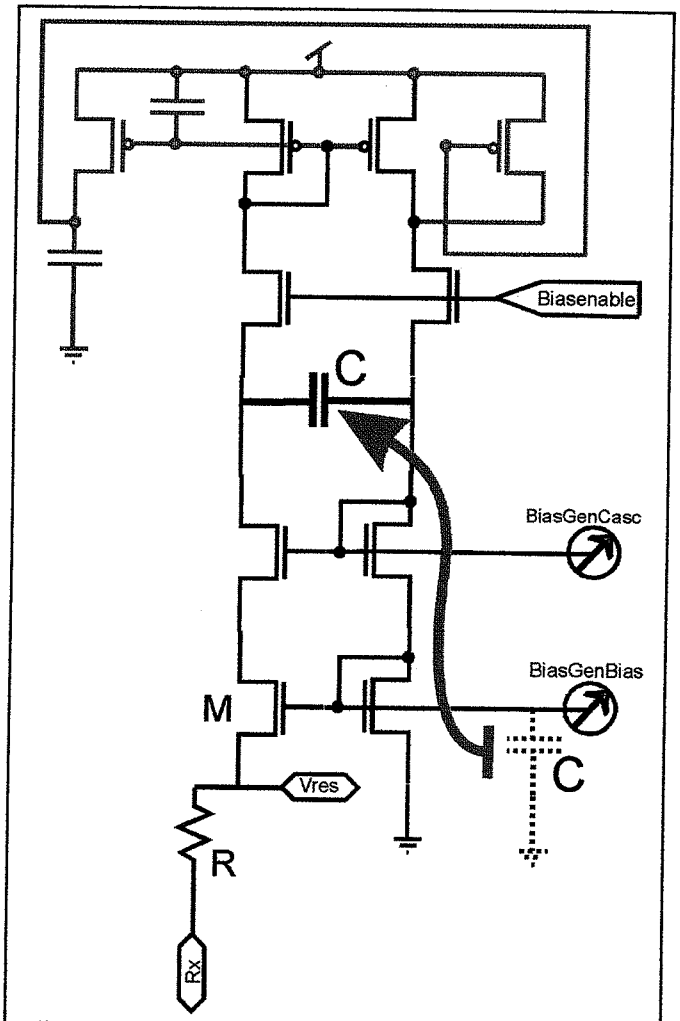

Figure 6.1: modification of the bias generator bias. The displacement of the capacitance C improves the stability of the circuit valuably and can be done without great changes in the layout of the chip.

To improve the performance of friend 10 and therefore to stabilize the masterbias the node nbias should be brought to a pin directly. This would allow to add capacitance to the gate of the n-fet mirror and so to obtain a ratio C_g:C_s which damps the oscillation. Secondly the capacitance C should be placed between the two sides of the circuit as a compensation as shown in figure 6.1. In this arrangement the oscillations of the p-fet gate and the n-fet gate would inhibit each other. Simulations with Analog and Tspice supported this proposition; the circuit was not oscillating even for a ratio C_g:C_s of thousand. The displacement of the capacitance in a new revised edition of the chip can be done easily, because the existing capacitance only has to be hooked to the new place.

References

C. A. Mead, *Analog VLSI and Neural Systems*

Script CNS and DNS

Klas Bult and Govert J. G. M. Geelen, *An Inherently Linear and Compact MOST-Only Current Division Technique*

E. A. Vittoz and X. Arreguit, *Linear Networks Based on Transistors*

Andreas G. Androu, Kwabena A. Boahen, Pilippe O. Pouliquen, Aleksandera Pavasovic, Robert E. Jenkins and Kim Strohbehn, *Current-Mode Subthreshold MOS Circuits for Analog VLSI Neural Systems*

Appendix

Matlab script for differential equations for two capacitors

Solve differential equations, higher order method.
ODE45 integrates a system of ordinary differential equations using
4th and 5th order Runge-Kutta formulas.

m-file: la21.m

```
%CALL THIS FILE IN MATLAB
%solve diff.equation in la2
%use solver different available (23, 45, 113,...) ('filename',[starttime,end
%time],[startvalue1,startvalue2])
global K Io Ipo Cg Cs Ut R M b c n m
K=0.8;
Io=1e-15;
Ipo=1e-15;
Cg=1e-13;
Cs=1e-10;
Ut=0.025;
R=1e5;
M=100;
b=Io/Cg;
c=Io/Cs;

hold on
%options=odeset('RelTol',1e-8);
for n=1:4
m=2*10^n;
b=(Io/(Cg*(m)));
```

```
f=n/20;
[t,y]= ode45 ('la2',0,0.6e-5,[0.8; 0.2],1.e-9);
plot(t,y)
end


%properties
title 'masterbias large signal behaviour'
xlabel 't'
ylabel 'V'
gtext('gate voltage')
gtext('source voltage')
```

m-file: la2.m

```
%CALL la21 IN MATLAB
%large signal behaviour model for transistors in subthreshld
%solve differential equation

function dy = F(t,y)
global K Io Ipo Cg Cs Ut R M b c n m

%input values y(1) is the gate voltage y(2) is the source voltage

%differential equation
dy = [exp(y(1)*K/Ut)*b*(M*exp(-y(2)/Ut)-1);(M*c)*exp((y(1)*K-y(2))/Ut)-
y(1)/(R*Cs)];
```

Matlab script for differential equations for three capacitors

m-file: la31.m

```
%CALL THIS FILE IN MATLAB
%solve diff.equation in mas1
%use solver different available (23, 45, 113,...) ('filename',[starttime,end
%time],[startvalue1,startvalue2])

global K Io Ipo Cg Cs Cm Ut R M b c d n m RR

                                %default values
K=0.8                             %0.8
Io=1e-15                           %1e-15
Ipo=1e-15                                  %1e-15
```

```
Cg=5e-12                                    %1e-12
Cs=1e-11                                    %1e-11
Cm=1e-13                                    %1e-14
Ut=0.025                                    %0.025
R=1e5                                %1e5
M=100                                 %100
b=Io/Cg
c=Io/Cs
d=Io/Cm
RR=R*Cs

hold on
%options=odeset('RelTol',1e-5);                    %set integration tolerance  1e-5
for n=0:3                                  %set # loops
m=10^n;                                    % set ratio of change
b=(Io/( Cg*m))                              %variable
%c=(Io/(Cs*m));
%d=(Io/(Cm*m));
                                          %,options
[t,y]= ode45 ('la3',0,21.11e-8,[0.7; 0.2; 4.2],1e-6,1);   %startvalues
[Vg=0.7,Vs=0.2,Vm=4]
%and timescale [0 1e-6]
plot(t,y);
end


%properties
title 'masterbias large signal behaviour'
xlabel 't'
ylabel 'V'
%legend('gate voltage', 'source voltage', 'p-fet gate voltage')
```

m-file: la3.m

```
%CALL la31 IN MATLAB
%large signal behaviour model for transistors in subthreshld
%solve differential equation

function dy = F(t,y)
global K Io Ipo Cg Cs Cm Ut R M b c d n m RR

%input values y(1) is the gate voltage y(2) is the source voltage y(3) is the p-fet gate
%differential equation

dy = [b*(-(exp(K*y(1)/Ut))+(exp(K*(5-y(3))/Ut))*(1-exp(-(5-y(3))/Ut)));
   ((c*M)*exp((y(1)*K-y(2))/Ut)-y(1)/(R*Cs));
   d*((exp(K*(5-y(3))/Ut))*(1-exp(-(5-y(3))/Ut))-M*exp((K*y(1)-y(2))/Ut))];
```