An Ultra Low Power Motion Detector

Diploma Thesis of Patrick Lichtsteiner

supervised by Dr. Tobi Delbrück
communicated by Prof. Rodney J. Douglas

Neuromorphic aVLSI Group
Institute of Neuroinformatics
ETH-University Zürich, Switzerland
patrick@ini.phys.ethz.ch

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Abstract

This diploma thesis presents a feasibility study and a completed layout for an ultra low power motion detector in standard CMOS technology. It describes the application, the circuits and its operation and implementation in CMOS technology. The report is divided in four chapters. Firstly the idea is introduced. Secondly the main circuit is presented and its operation discussed. The receptor circuit, the antibump circuit, the threshold circuit and the biasgenerator circuit are discussed in detail. The third chapter is dedicated to the architecture of the chip. Finally guidelines for the testing of the chip are provided and outlooks to a commercial application are given.
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Chapter 1

Introduction

1.1 The idea

Imagine a long hallway with doors opening into it from both sides. Further imagine a busy, absent minded person hurrying down this corridor. This person, for example a scientist, is in deep thought walking by closed office doors of his colleges. Suddenly the scientist, let us call him Tobi, is confronted with an unexpected event, he is hit by an opening door frame into the face. The person opening the door, thinking only of a hot coffee, notices only too late what harm she did. But how could she know?

The goal of this diploma thesis is to make a feasibility study for a device preventing such accidents. This device should warn a person opening a door that there is someone rushing down the hallway. It is required to be small, cheap and easy to install. It should reliably detect motion on either side of the door. If it detects motion on both sides of the door that is correlated, it should generate a visible or audible output, to warn the person opening the door. It should run for a year on one battery or should use a solar cell.

1.2 Why CMOS

This requirements are met by an ultra low power motion detector in CMOS technology. The advantage of this technology is the ability to combine image sensing and signal processing on the same chip. It is possible to design a single purpose chip which is very cheap in mass production and that requires only a few inexpensive external components. Really low power chips, like the ones in watches, are able to work for a long period on a single small battery. This obviates expensive wiring around the doors and makes the device autonomous. With a photo-voltaic cell it should be able to run totally
independent.

1.3 The circuitry

The circuit has to detect motion in very different lighting conditions. It must work with a dynamic range up to 4 decades of magnitude of illumination. It must not be affected by high contrast backgrounds and changes of the lighting conditions. Therefore I chose to use the adaptive receptor circuit of T. Debrück and C.A. Mead [5]. It detects transient changes in photo current. If used with high gain the receptor acts like a differentiator of the photo current with a voltage output and steady state voltage offset. The adaptive receptor circuit needs a bias current to run. This master current must adapt itself to the lighting conditions to minimize power consumption.

Every pixel has its own receptor circuit. If the overall lighting conditions change, every pixel generates a voltage peak. To prevent the chip from confusing such an event with motion, the outputs of the different pixels have to be compared. The outputs are compared relative to each other by using an antipump circuit which measures the absolute value of the difference of the output voltage of its own pixel and the average output voltage of all the pixels. The antipump circuits generate current outputs which are summed up and differentiated in a modified receptor circuit. A threshold stage at the end transforms the output voltage of the modified receptor into an digital output signal. It is crucial to use a special circuit to threshold because the normal digital inverters consume a lot of power while switching.

The whole motion detector is composed of two chips, some off chip components as the power source, a beeper and a LED and lenses. The outputs
of the chips are hooked to a correlator unit on one of the chips via a flat flex cable around the door frame. Figure (1.1 c) shows the whole device. To minimize the off chip components, the bias currents are generated on chip. This is achieved with the bias generator circuit used by T. Delbrück on the physiology helper chip [6].

1.4 What is new

Most of the circuits used for the ultra low power motion detector are widely known. The photodiode and the adaptive photoreceptor circuit was thoroughly presented by T. Delbrück and C.A. Mead [5]. The photoreceptor circuit has been used many times in interesting neuromorphic designs. The antibump circuit has been introduced by Delbrück [7]. The follower-aggregation network is presented in C.A. Mead’s book *Analog VLSI and Neuronal Systems* [11].

The ultra low power motion detector is a novel approach to detect motion. The use of a set of adaptive photoreceptor, whose changing signals are further adaptively amplified, leads to a sensitive and stable detector. I add a novel feed back to the photoreceptor circuit to reduce the power consumption by adaptation to the lighting conditions. Furthermore I introduce a novel threshold stage which is optimized for low power consumption and which is only dependent on ratios of currents for manufacturing stability.

The diploma thesis presents the main circuit and discusses its operation. The receptor circuit and its adapted power consumption, the antibump circuit, the threshold circuit and the bias generator circuit are explored in detail. The third chapter describes the layout of the chip. Because it was not possible to design, fabricate, test and assemble the whole device in the duration of 4 months, the thesis proposes how to test the chip and gives some outlooks to a possible commercial application.
Chapter 2

The circuit

Figure (2.1) shows a schematic of the core which includes all the circuitry of the chip but the pads. The centerpiece of the core is the pixel. It consists of the adaptive receptor circuit, a follower and an antibump circuit. Every pixel is connected to a photodiode which generates the input current to the receptor circuit. The core is built up of thirty pixels, a feed back circuit to control the bias current of the adaptive receptor, an adaptive receptor circuit, called summadap circuit, summing up the anti bump currents, an output stage, built up of two threshold circuits and a delay circuit, a correlator circuit and a bias-generator circuit.

2.1 The photo sensor

In 1905 Einstein published his famous thesis about the photo electric effect. He said that if a photon hits an atom it can be absorbed by lifting an electron into a higher energetic state. In the solid state physics this means that an incident photon can excite an electron into a higher energetic band. This knowledge was applied to semiconductors in order to detect photons with silicon. If a photon carries enough energy it can excite an electron from the valence band into the conduction band and therefore create an electron-hole pair.

The energy needed for the generation corresponds to the band gap energy $E_g$. Photons with lower energy will not create any electron hole pairs. Thus it is important to choose the right material for photo detection. Silicon meets this requirement for visible and near-infrared light.

There are different ways used to build photo sensors. The market of image-sensors is dominated by the so called charge coupled devices (CCD). CCD sensors are fabricated in processes that are not compatible to standard
Figure 2.1: The core of the circuit: a) photodiodes, b) pixel, c) low power circuit, d) bias-generator circuit, e) summadap circuit and f) threshold stage
CMOS technology. Standard CMOS technology based sensors are usually photodiodes.

2.1.1 Photodiodes

A photodiode is a normal p-n junction used as a photo sensor; a possible implementation is displayed in figure (2.2 a)). Since the diode is part of every transistor, photodiodes are available in standard semiconductor processes.

Illumination of a semiconductor increases the concentration of the mobile charge carriers by creation of electron-hole pairs. This process is counter-balanced by recombination due to diffusion in equilibrium. In the presence of an electric field the carriers tend to be separated. This happens in the depletion region of a p-n junction. If an electron-hole pair is generated within the diffusion length of the depletion region, the carriers are influenced by the built-in electric field near the junction. The electrons drift into the n-region while the holes are attracted by the p-region, as shown in figure (2.2 b)).

This leads to a reverse current through the diode which is called the photo current. The photodiode allows different modes of operation. It can be used to convert optical power into electrical power or as a photo sensing device. In the photo sensing mode, the photodiode is either open-circuited or reverse biased. If the diode is open-circuited the generated current builds up a potential which forward biases the diode until steady state is attained. Steady state means that the forward diffusion current balances the photo current. The potential is then read out. If the diode is reverse biased, the reverse current is read out.

The amount of the reverse current can be estimated as a function of
CHAPTER 2. THE CIRCUIT

photon incidents via the quantum efficiency $Q(\lambda)^{1}$. T. Delbrück and C.A. Mead \cite{5} estimated the current for a 10\(\mu\m) \times 10\(\mu\m)\) photodiode area with a quantum efficiency of 0.5 under 1\(W/m^{2}\) irradiance, which corresponds to typical office fluorescent lighting conditions, as:

$$\frac{1}{sm^{2}} \cdot \frac{eV}{1.6 \cdot 10^{-19} J} \cdot \frac{Q}{2.5eV} \cdot (10\mu m)^{2} \cdot 0.5 = 10^{8} \frac{Q}{s} = 25pA. \quad (2.1)$$

The lighting in a hallway is less than office lighting and the walls do not perfectly reflect light. The irradiance onto the photodiode is further reduced by the optics by a factor of:

$$\frac{1}{4f^{2}}; \quad \text{where} \quad f = \frac{\text{aperture}}{\text{focal length}}. \quad (2.2)$$

The estimation points out that photodiodes generate very small currents in the range of \(fA\) up to \(nA\). It is difficult to directly supply current for active circuits from photodiodes. There are different ways to transform the reverse current of a photodiode into a voltage. Simple logarithmic photo sensors convert the current, with one or two transistors in series with the diode, into a voltage. This voltage is logarithmically dependent on the current giving the sensor a large dynamic range. With a feedback loop the voltage across the diode can be clamped. This increases the bandwidth of the photo sensor further. Such applications must contend with a large mismatch in the DC outputs.

2.1.2 The adaptive logarithmic photoreceptor

The logarithmic adaptive photoreceptor is a good choice for a motion detector, because it has low gain for static signals and high gain for transient signals that are centered around the adaptation point. The version of the receptor used for this chip was first published and discussed in detail by T. Delbrück and C.A. Mead \cite{5}.

The power consumption of the chip is dominated by the photoreceptor. Therefore the discussion here will focus on the engineering trade offs required for ultra low power operation, in particular the novel adaptive biasing.

\footnote{The quantum efficiency is defined as

$$Q(\lambda) = \frac{\# \text{ collected charges}}{\# \text{ incident photons at wavelength}(\lambda)}$$

and is largely frequency dependent. T. Delbrück and C.A. Mead \cite{5} published measured spectral quantum efficiencies for different diode types.}
A biological concept

The circuit is biologically inspired. The characteristics adopted by the silicon version of the biological original are the adaptive properties, the gain control resulting in illumination-independent contrast response, and the invariance of the response time to illumination [5]. Similar to the biological system, the photoreceptor circuit pre-processes the photo current locally before any sampling or long-range communication takes place.

The adaptive receptor can be described as a biological concept. Therefore it is divided in four parts as showed in figure (2.3). An internal Model is used to predict the Input. The prediction is then compared to the Input. The Comparison generates the output and refines the model by Learning. The adaptive receptor circuit implements a simple type of learning by its adaptation.

IC implementation

The input stage of the receptor is implemented by a reverse biased photodiode, as shown in figure (2.3). The source voltage $V_p$ of the feedback transistor $M_{fb}$ depends logarithmically on the photo current since the transistor oper-
ates for typical irradiation intensities in subthreshold. The voltage difference stored between $V_p$ and $V_{fb}$ on the capacitance $C_1$ drives the model current in $M_{fb}$. The comparison is modeled with an inverting amplifier consisting of the two transistors $M_{pAmp}$ and $M_{nAmp}$. A pFET with its gate and drain connected to $V_{fb}$ and its bulk and source connected to $V_{out}$ performs the adaptation.

The response of the circuit to a small increase of the photo current illustrates the basic function of the circuit. The voltage $V_p$ is pulled down. In reaction the output voltage $V_{out}$ goes up $A_{amp}$ times as much. The output change is fed back to the gate of $M_{fb}$ through the capacitive divider. The increased gate voltage pulls up $V_p$. The voltage $V_p$ is now at about the same voltage as it was in the beginning. Instead of moving the source voltage of the feedback transistor its gate is moved. This happens because the feedback amplifier has a much higher gain than the gate-source of $M_{fb}$ and the capacitive divider formed by $C_1$ and $C_2$. The adaptive receptor clamps the voltage across the photodiode and therefore increases its bandwidth.

The adaptive element in this circuit, known as the expansive element or Tobi element [5], has non-linear properties. It acts like a pair of diodes in parallel with opposite polarity. If the voltage across the element is small it has a very high resistance. With increasing voltage the current grows exponentially.

### The photoreceptor gain

The gain of the photoreceptor is easy to compute for the case that $A_{amp}$ is large and the adaptive element is not taken into account. The current through the feedback transistor $M_{fb}$ has to equal the current through the diode. For steady state this means that the linearized small signal gain for a change in photo current $\Delta I_{bg}$ relative to a starting level $I_{bg}$ is given by

$$\frac{\Delta V_{out}/U_T}{\ln(1 + \Delta I_{bg}/I_{bg})} = \frac{1}{\kappa}.$$  \hspace{1cm} (2.3)

The transient gain takes into account the capacitive divider formed by $C_1$ and $C_2$. The linearized transient gain, called $A_{cl}$, is

$$A_{cl} = \frac{\Delta V_{out}/U_T}{\ln(1 + \Delta I_{bg}/I_{bg})} = \frac{1}{\kappa} \frac{C_1 + C_2}{C_2}.$$  \hspace{1cm} (2.4)

Equation (2.3) displays the logarithmic properties of the adaptive receptor circuit. The differences between equation (2.3) and (2.4) show that the ratio of the gains is adjustable by the capacitive divider ratio $(C_1 + C_2)/C_2$.

---

2cl is used as a short cut for closed loop
The response of the circuit to a constant $\Delta I_{bg}/I_{bg}$ does not depend on the background current.

With a large $C_1$ compared to a minimal $C_2$ the receptor is very sensitive to transient changes of the photo current even if the changes are slow. This behavior, as shown in figure (2.4), is desired to detect changes of brightness and therefore also motion. The lowest trace shows the input current and the upper traces are the output voltages for different bias currents $I_b$. After peaking in response to a steep slope in the input, the output decays logarithmically to its steady state value over a timescale of several seconds. The non ideal behavior is that $V_{out}$ rings or even worse, that it lags behind.

Because the adaptive receptor uses active feedback, the stability of the circuit has to be explored. The small-signal analysis of the adaptive photoreceptor is available to the interested reader in Delbrück’s photoreceptor paper [5]. Results which are used later are summarized in the following paragraph.
Stability discussion

The adaptive photoreceptor circuit is a third order system if adaptation is considered. The adaptation time constant is so large compared with other time constants that for most purposes it can be neglected. The resulting second order system, which will be called the transient transfer function of the receptor is

\[
H(s) = \frac{A_{cl}}{(A_{cl}/A_{amp})(\tau_{in}s + 1)(\tau_{out}s + 1) + 1},
\]

where \(A_{amp}\) is the voltage gain of the inverting amplifier. It is determined by \(g_m/g_{out}\):

\[
A_{amp} = \frac{\text{transconductance of } M_n}{\text{output conductance of the amplifier}} = \kappa \frac{1/U_T}{1/(1/V_{E_n} + 1/V_{E_p})},
\]

where \(\tau_{in}\) and \(\tau_{out}\) are the time constants of the output and input node respectively and the \(V_E\) are the Early voltages of the amplifier transistors. The time constants are calculated by the following equations:

\[
\tau_{in} = \frac{C_{input}U_T}{I_{by}}, \quad \tau_{out} = \frac{C_{amp}}{I_b} \frac{1}{V_{E_p} + 1/V_{E_n}}.
\]

To study the second-order temporal behavior the transfer function of the receptor is compared to a canonical form for a transfer function of a second order system \(^3\)

\[
H(s) = \frac{1}{\tau^2s^2 + \frac{\tau}{Q}s + 1}.
\]

The system is critically damped for \(Q = 1/2\). From (2.5) and (2.8) \(Q\) and \(\tau\) are written as:

\[
\tau = \sqrt{\frac{\tau_{out}\tau_{in}}{A_{loop}}}, \quad Q = \sqrt{A_{loop}} \sqrt{\frac{\tau_{out}\tau_{in}}{\tau_{out} + \tau_{in}}} \quad \text{where} \quad A_{loop} = \frac{A_{amp}}{A_{cl}}
\]

Now a criterion for critical damping of the adaptive photoreceptor is easily found:

\[
Q \leq 1/2 \quad \text{when} \quad \tau_{out} \leq \frac{1}{4A_{loop}}\tau_{in}.
\]

\(^3\)This method is beautifully described in C.A. Mead’s book Analog VLSI and Neural Systems \(^{11}\).

\(^4\)“1/\(\tau\) is the radius of the circle on which the poles sit, and \(Q\), stated loosely, is the number of cycles of ringing in response to a step input.” \(^{5}\)
For a critically damped response the time constant at the output of the inverting amplifier has to be smaller than the time constant of the input node by a factor of four times the loop gain. The time constant $\tau_{out}$ is determined by (2.7). It is influenced by the early voltages of the transistors in the inverting amplifier $V_{E_n}$, $V_{E_p}$ and the bias current $I_b$. The input time constant $\tau_{in}$ is proportional to the inverse photo current $1/I_{bg}$. The loop gain also depends on the early voltages $V_{E_n}$ and $V_{E_p}$ as shown in (2.9) and (2.6). The closed loop gain, which also influences the loop gain, is determined by the capacitive divider.

Interrelation between gain, power consumption and stability

In summary, the receptor is tunable by the Early voltages (which are proportional to the respective transistor lengths) the bias current $I_b$ and the capacitive divider ratio. The requirements to be met for a low power motion detector are a high transient gain, wide dynamic range, small bias current and reasonable stability.

The gain of the amplifier is calculated from equation (2.6). The early voltages for the AMS 0.8 $\mu$m process for a transistor length of 6$\mu$m is around 200V$^5$. The gain of the designed amplifier for $\kappa = 0.7$ is about 2800.

To achieve a high sensitivity even to small transient changes in photo current the capacitive divider ratio is chosen high. This has a positive effect on the stability because it leads to a large closed loop gain $A_{cl}$. The effective values used are $C1 = 3.72pF$ and $C2 = 10.1fF$ and with equation (2.4) $A_{cl} \approx 530$.

There is one variable and one equation left. It is the bias current and the criterion for critical damping of the photoreceptor circuit. Therefore it is possible to relate the bias current $I_b$ directly to the photo current $I_{bg}$:

$$Q \leq 1/2 \quad \text{when} \quad I_b \geq \frac{1}{U^2 T A_{cl}} \cdot \kappa \cdot V_E^2 \cdot I_{bg} \approx 85000 \cdot I_{bg}.$$  \hspace{1cm} (2.11)

If the photo currents are in a range of 1$pA$ to 1$nA$ the bias current would have to be permanently over 85$\mu$A to satisfy the stability criteria for the whole range. This current is way out of low power for a single receptor and would total for 30 pixels to about 2.55mA.

The circuit needs not necessarily be damped critically because the maximum amount of ringing is low. By searching for the extremes in (2.9) the condition for maximum $Q$ is obtained [5]:

$$Q = 1/2 \sqrt{A_{loop}} \approx 1.2 \quad \text{when} \quad \tau_{out} = \tau_{in}. \hspace{1cm} (2.12)$$

$^5$This data was read out of a least square fit to the measured conductances, published by Shi-Chii Liu [10](p.73)
Because the poles of the transfer function of the receptor have all negative real part, as shown in the root locus plot (2.5), the output voltage will not oscillate even for very small ratios $I_b/I_{bg}$.

In the application for a low power motion detector the bias current is therefore not mainly determined by stability but by power consumption and bandwidth. The time constant $\tau_{out}$ has to be small enough to resolve transient changes induced into the photo current by a moving person. Simulations in Analog\footnote{Analog is a simple but easy to use circuit simulator designed by John Paul Lazzaro [8]} and Tspice\footnote{Tspice is a circuit simulator distributed by Tanner Tools, www.tanner.com} pointed to a ratio of $I_b/I_{bg}$ of about 300 as an agreeable compromise between power consumption and bandwidth. A Tspice simulation is shown in figure (2.4). The output node of the receptor circuit is hooked up to $C1$ and to two gates (see section(2.2)), and has to drive a capacitance of approximately $100fF$. Biases that are too small will filter out even slow changes in photo current. In section (2.3) I will discuss the adaptive biasing of the photoreceptor.

2.2 The pixel’s motion energy computation

In figure (2.1 b)) the pixel is presented. It is built up of the photoreceptor, a unity gain-connected transconductance amplifier and an antibump circuit [7].

The pixel is the main processing unit of the circuit. The input of every pixel is the photo current of its photodiode. The output is a current which is
a measure for the dissimilarity between the output voltage of its own receptor and the average of the output voltages of all the receptors.

This architecture allows distinguishing between motion and overall light changes in the following way: If the overall lighting conditions change, all photo currents change by the same ratio and there is no change between the direct output voltages of the receptors and their average. If a person walks through the receptive field of the chip only a few photo currents change. The pixels affected by the changes produce large dissimilarity current outputs.

The easiest way to average voltages is to hook each of them to a common node through a common value of conductance. Because the output voltage of the photoreceptor is further needed and is used in the local feedback, it is copied through a follower circuit. The copied voltages are then tied together to form a follower aggregation circuit\(^8\)\(^9\).

The dissimilarity of the common node and the output node of the photoreceptor is computed in the antbump circuit shown in figure (2.6). The

\(^8\)The Deworth-Mead follower-aggregation circuit is discussed in C.A. Mead’s aVLSI book [11] on p.105/106. The voltage of the output node of the follower aggregation circuit is calculated as follows:

\[
V_{out} = \frac{\sum_{i=1}^{n} G_i V_i}{\sum_{i=1}^{n} G_i}.
\]

\(^9\)The follower-aggregation network acts here like a retinal horizontal cell.
subthreshold current \( I_{\text{mid}} \) through transistor \( M_4 \) and \( M_2 \) is [7]:

\[
I_{\text{mid}} = \frac{I_b}{1 + \frac{4}{3} \cosh^2 \frac{\kappa \Delta V}{2}} \quad \text{where} \quad \Delta V = V_{\text{in1}} - V_{\text{in2}}.
\]  

(2.13)

The dissimilarity current output of the antibump circuit is the sum of the currents \( I_1 \) and \( I_2 \), calculated with Kirchhoff’s current law,

\[
I_1 + I_2 = I_b - I_{\text{mid}}.
\]

(2.14)

The transistor strength ratio \( S^{10} \) controls the fraction of the bias current \( I_b \) that is supplied by \( I_{\text{mid}} \) if the input voltages are equal. \( S \) also sets the width of the antibump. Delbrück calculates the width at \( e \) times the minimum value of the antibump and obtains:

\[
\Delta V_{1/e} \approx U_T \frac{2}{K} \ln S \quad [7].
\]

(2.15)

For \( S = 21 \) the width at \( 1/e \) is approximately 220mV. Delbrück stated [7] that the calculations fit the measured data quite well with the exception that the fabricated circuits acted as though \( S \) was much larger than expected from the drawn value [7]. The antibump circuit used for this chip has width/length ratios of 36/6 and 6/21 for the inner and the outer transistors respectively.

The bias current \( I_b \) is approximately the maximum value of the antibump current \( I_1 + I_2 \) and also current limits the whole circuit. The higher the bias current, the higher the antibump currents become, see figure (2.6). If the currents are large the signal to noise ratio increases. But high bias currents have the disadvantage of a higher power consumption. This has to be considered because the bump circuit is used thirty times. The antibumps on the chip consume 32nA. This proved to be sensitive enough in the simulations and forms only a small fraction of the power consumption of the whole chip.

2.3 The adaptive bias circuit for the photoreceptor

As shown in section (2.1.2), a ratio \( I_b/I_{bg} \) of approximately 300 is desired. The novel low power circuit maintains this ratio for different photo currents. The input of the circuit is the sum of the photo currents of all the diodes taken from the drains of the transistors \( M_f \) of the receptor circuit (see figure

\(^{10}S = (W_{\text{mid}}/L_{\text{mid}})/(W_{\text{outer}}/L_{\text{outer}})\)
Figure 2.7: The adaptive bias circuit for the photoreceptor. The input to the circuit is the sum of the photo currents of the photodiodes taken from the drains of the transistors $M_{fb}$ of the 30 receptor circuits (see figure (2.3)). It is mirrored with a gain of 10 to the right resulting in a receptor bias current 300 times the average photo current. The gate voltage of the pFET on the right side is then used to bias the photoreceptor. The off-chip capacitor and the source follower bias allow adjustment of the time constant of the bias current adaptation.

The output of the circuit is the bias current for the receptor circuit. The circuit is displayed in figure (2.7).

The 30 summed photo currents are mirrored with a gain of 10 from the input to the output, resulting in an overall ratio of 300. Instead of using a diode connected nFET, a source follower circuit is implemented in the low power circuit. The result is that the adaptive bias circuit’s time constant $\tau_{adap}$ is adjustable.

The time constant is composed of the off chip capacitance $C_{of\_chip}$ and the conductance of the source follower circuit, which is dominated by the source conductance of $M_f$. It is calculated as:

$$\tau_{adap} = \frac{C_{of\_chip}}{I_b} \cdot U_T.$$  \hspace{1cm} (2.16)

Because the low power circuit is an additional feedback to the photoreceptor, its time constant should be widely separated from the time constants of the receptor (in particular the receptor adaptation) to prevent instability. For $\tau_{adap} = 10s$ and the bias current $I_b = 16nA$ the off chip capacitance has to be 6.4$\mu F$. 

(2.3).
2.4 The summadap circuit

The *summadap* circuit is another photoreceptor circuit which has the summed antibump currents as inputs instead of a photo current. The circuit is the same as the photoreceptor circuit except for a larger capacitance $C_2$ that increases the adaptation time constant. Furthermore to the output voltage $V_{out}$ of the circuit is added another output voltage, called $V_{Ad}$. The voltage $V_{Ad}$ does not move around as much as $V_{out}$ does due to the adaptive element. In steady state the two nodes are very close while they differ for transient signals.

The adaptive behavior of the circuit is used to detect only changes in the summed antibump current. The voltage $V_{out} - V_{Ad}$ is an amplified representation of the motion signal that discords the DC component of the summed antibump currents (see figure (2.10)). This is nice because the circuit produces not only a high response to transient signals but also a reference to subtract the steady state offset voltage.

2.5 The threshold stage

The novel threshold stage is used to convert the analog voltage signals out of the summadap circuit into a digital output voltage, with high implying motion and low if nothing is moving. Furthermore the output voltage should stay high for a short time after motion was detected.

All thresholds arise from ratios of currents which is crucial for manufacturing and operating reliability.

The threshold stage consists of three circuits in series as visible in figure (2.1). Firstly the output voltages of the summadap circuit $V_{out}$ and $V_{Ad}$ are checked for dissimilarity in the *antibump threshold* circuit. Secondly the outputs of the antibump threshold circuit are stretched in time with the *delay* circuit and the *low power threshold* circuit. The schematics of the three circuits are displayed in figure (2.8).

The antibump threshold circuit

The antibump threshold circuit thresholds the dissimilarity voltage $\Delta v = v_{out} - v_{Ad}$. It is built up like a simple bump circuit, published by T. Delbrück [7], with the similarity output \footnote{The similarity output is the current running through the middle tree of the circuit. It has its name because of the response of the circuit, which peaks for $\Delta V = 0$, see also [7].} tied to a nFET, thus forming an inverting amplifier (composed of $M_1$ and $M_5$). The output of this inverting amplifier is
tied to the pFET of another inverting amplifier (composed of $M_6$ and $M_7$) which is biased with a current that is a fixed ratio of the circuit bias current. The similarity current $I_{mid}$ is calculated as follows,

$$I_{mid} = \frac{I_b}{4 \cosh^2 \frac{\kappa \Delta V}{2}} \quad \text{where} \quad \Delta V = V_{in1} - V_{in2}, \quad (2.17)$$

if the two inverting amplifiers are not taken in account. The gain of both of the inverting amplifiers is determined by the Early voltages of the transistors forming them. The nFETs are biased with the node $thOut$ while the currents through the pFETs change in response to the changes of the similarity current. The gain of an inverting amplifier with the pFET gate as input terminal is computed as follows:

$$A_p = \frac{\partial V_{out}}{\partial V_{sp}} = \frac{\kappa}{U_T} \frac{1}{\frac{1}{V_{Ep}} + \frac{1}{V_{En}}}. \quad (2.18)$$

This gain is around 2800 for Early voltages around 200V. Therefore the output voltage of the inverting amplifiers are pulled very close to the rails for small differences between the currents $I_{mid}$ and the bias current $I_{b_{out}}$ determined by $thOut$. If $I_{mid}$ is larger then $I_{b_{out}}$ the output voltage $V_{out}$ is close to ground. When $I_{mid}$ equals $I_{b_{out}}$, $V_{out}$ switches from one rail to the other. The output voltage $V_{out}$ of the circuit as a function of the voltage difference $\Delta V$ has the form of a “rectangle antibump” as displayed in figure (2.9 a)).

Figure 2.8: a) antibump threshold circuit, b) delay circuit c) low power threshold circuit
Figure 2.9: The left plot displays the response of the antibump threshold circuit to sine wave input. The plot on the right shows the width of the antibump as a function of the bias current ratios. The blue line is the calculated curve for $S = 2$, the green curve is the result of a calculation with $S = 3.5$ (see equation (2.19)) and the red circles mark the simulation results for $S = 2$ (Tspice BSIM3v3 level 49).

Because the antibump threshold output switches when $I_{\text{mid}} = I_{\text{b, out}}$, the width of the rectangle antibump is determined by the following equation in terms of the voltage difference $\Delta V$:

$$2 \cdot \Delta V = \frac{2}{\kappa} \cosh \left( \frac{I_b S}{4 I_{\text{b, out}}} \right).$$

(2.19)

The half width of the antibumps as a function of the ratio of the bias currents $I_{\text{b, out}}/I_b$ for $S = 2$ is plotted in figure (2.9 b)). The blue line displays the calculated values, the green line is a theoretical fit with $S = 3.2$ to the Tspice simulation values marked as red dots. The antibump threshold circuit acts in the simulation as if the $S$ values were significantly larger than drawn (compare to the statement of T. Delbrück mentioned in section (2.2)).

The delay circuit

The delay circuit is a source follower circuit with a strong nFET at the input and a weak nFET at the source. To the output node a capacitance is tied off-chip. This leads once more to an adjustable time constant which depends on a bias current and a capacitance.

Essentially the delay circuit is a peak detector with controllable retention time. It is important to mention that the time constant depends on
the direction of the voltage change at the input. Rising voltages are linked to a small time constant whereas decreasing voltages go with a large time constant. This behavior allows delaying the output-decay for an adjustable time.

The low power threshold circuit

The output of the delay circuit is not digital anymore and therefore needs to be compared to a threshold one more time. This is done by the low power threshold circuit. It is built like the antibump threshold circuit but loses the transistor $M_5$ as shown in figure (2.8 c)). The resulting behavior is rather that of a differential-pair circuit than that of the antibump circuit. The current through the pFET $M_3$ follows the current through $M_2$ with a ratio of $S$.

The output voltage of the delay circuit is fed into the $in1$ node becoming the input voltage of the threshold circuit. To the other input node a reference or threshold voltage is applied. If the input voltage is bigger than the reference voltage the output of the threshold circuit is close to Vdd, otherwise it is near ground. A lot of different voltages are generated in the bias generator and brought to pins. The threshold voltage can be selected by tying the appropriate pin back.

Figure (2.10) shows a Tspice simulation of the core. The current input to all the receptor circuits was constant but for one which is displayed as dashed line. The dotted trace shows the threshold voltage applied to the low power threshold circuit. The antibump threshold output is colored green, the delay output red and the low power threshold output blue.

Advantages and disadvantages of the novel threshold stage

The nice thing about the threshold stage is that its power consumption is limited by the bias currents. This is very important for a low power device converting analog voltages into digital voltages, because often the inputs do not change very fast leading to huge currents through normal inverters.

The antibump threshold and the low power threshold circuits are very useful for comparing slowly changing voltage signals to references. They function over a wide range of inputs and their references or thresholds can be easily adjusted. The drawback of the circuits compared to common threshold circuits is that it uses current all the time, not only while switching. This constant power consumption is severe if the circuits should have short time constants, because the time constant is inversely proportional to the bias currents.
Figure 2.10: Transient analysis of the core (Tspice BSIM3v3 level 49). The uppermost plot shows the low power threshold output. The second one displays the traces delay output (red), antibump threshold output (green) and the threshold voltage (dotted). The summadapAd voltage (green) and the summadapOut voltage (blue) are shown in the third plot and the input current in the lowest plot.
2.6 The bias generator

The bias generator circuit supplies the bias currents and reference voltages needed on chip. It is built up of a masterbias that sources a controlled, steady reference current, a current divider network that divides down the reference current by two every stage, and circuits that generate the needed biases from the references. The bias generator circuit was used by T. Delbrück the physiology helper chip [6].

The version for this chip uses a slightly modified masterbias circuit \(^{12}\). The modification concerns the displacement of a capacitance to optimize the stability of the circuit, which I proposed in my semester arbeit [9]. The masterbias is shown in figure (2.11). The master current is set from off-chip with the value of \( R \) according to the following equation:

\[
I_{\text{master}} = \frac{1}{R} U_T \ln(M) \quad R = \frac{1}{I_{\text{master}}} U_T \ln(M) \quad (2.20)
\]

The master current flows through two diode connected nFETs where it originates the GenNCasc and the GenNBias voltages. The additional pFETs and the 2 capacitors form a start up circuit invented by Tim Allem of Synaptics Inc. \(^{14}\).

\(^{12}\)See reference [12] for basic description of the CMOS version of Widlar’s classic bipolar bootstrapped current mirror current source

\(^{13}\)where \( M \) is the relative \( W/L \) shown in figure (2.11 a))

\(^{14}\)http://www.synaptics.com/
The nbiassource circuit mirrors the master current to a pFET using the GenNCasc and the GenNBias node. This procedure is profitable because the p-type transistors source a current independent\textsuperscript{15} of the drain voltage. This current is then pushed into the current divider network.

The current divider network [3] is designed to divide the current every stage by two, generating an array of reference currents. To transform the currents into voltages, they each flow through a diode connected nFET, whose source is connected to ground. The gate voltages are available to reconstruct the reference currents in any equal sized nFET with the same source voltage.

Such a gate voltage is then picked out and mirrored with another nbiassource circuit to a circuit that divides or multiplies the current to its required value.

The master current selected for this chip is 128\textit{n}A. The current divider network supplies 128\textit{n}A, 64\textit{n}A, ..., 1\textit{n}A. The bias currents used for the circuits are either equal, three times higher or three times lower then one of these.

The use of a bias generator circuit on chip allows building devices which need very little wiring and off chip elements. This benefits the handling of a chip and lowers the costs for a product dramatically.

2.7 The Test chip

Calculations and simulations are the basic tools to predict the operation of a chip, but only measurements on a fabricated device prove if the design works.

To actually test the circuitry described above, I designed a test chip. The test chip has some more features then a production version. It is important to have access to the crucial points in the circuit to observe the behavior and also to influence or overdrive signals. It is also helpful to have some pieces of the circuit duplicated separately on the chip to have access to isolated measurements.

The test chip has thirty pixels, a summadap circuit, a low power feedback, a bias generator circuit and three threshold stages with different sensitivities. Furthermore some stand-alone circuits are included, an antibump threshold circuit, an adaptively biased photoreceptor circuit, a nFET and a pFET in the standard size\textsuperscript{16} used for all the bias transistors and a correlator circuit which produces large driven outputs enabling direct connection to LEDs or buzzers. The detailed schematics are included in the appendix (A.2).

\textsuperscript{15}According to the basic subthreshold equations the current in saturation is determined by the gate and the source voltage only. Cascoding further reduces the Early effect.

\textsuperscript{16}The "standard" sized transistor is defined in section (3.2).
Chapter 3

The Architecture

3.1 The Process

To produce a small quantity of chips it is possible to share a wafer with other people. Austria Micro Systems (AMS) offers multi project wafers (MPW) manufacturing runs. The chip is designed for the AMS 0.8\(\mu m\) CYE process. The smallest area available is 5\(mm^2\) and the corresponding package has 64 pins. The process provides the following mask layers\(^1\):

- **ntub** ntub layer, well, a lightly ntype doping
- **diff** diffusion layer, area specification for nplus and pplus doping
- **nplus** n+implant layer, higher n doping for drain, source for nFETs and well contacts
- **pplus** p+implant layer, higher p doping for drain, source for pFETs and substrate contacts
- **poly1** poly 1 layer
- **poly2** poly 2 layer
- **met1** metal 1 layer
- **met2** metal 2 layer
- **cont** contact layer, connects metal 1 to diff, poly1 and poly2
- **via** via layer, connects metal1 to metal2
- **pad** pad layer, specifies surfaces not to be over-glassed (also used as 'photo layer')

\(^1\)mask layers are the basic definition layers fundamental to the construction of IC elements.
3.2 The chip architecture

The pad-frame and the pads used for this chip were designed and tested by different members of the neuromorphic aVLSI group. The area inside the minimum pad frame is about 1600µm by 1600µm. That is much more than needed for this design.

Because space was not crucial for this project, I choose the “standard” lengths and widths of a square transistor to be 6µm by 6µm. In not using the narrowest and shortest transistors, effects of device mismatch are reduced. A lot of guard structures are place around the circuitry and the diodes to reduce the effect of electron-hole pairs created by photons. All the circuits are carefully covered with metal 2 to omit direct irradiance.

In figure (3.1) the whole layout of the chip is displayed. In the center of the picture, the photodiodes are visible. The spacing of the diodes is chosen to have equal resolution over the whole receptive field of the device. The diodes are small, long and far spaced from each other. This means that the chip is blind but for small slits. The advantage of this design is that a photo diode’s receptive field is completely covered by a passing person, and therefore more change in the photo current is induced. The area of the ntub layer is about 1600µm². With office lighting and without lenses and a quantum efficiency of about 0.5, the photo current of the diode would be around 400pA. With the lenses and considering not looking at a white surface, the current is likely to be two decades smaller.

Under the diodes the array of 30 pixels is placed. The pixels are designed long and slender. They are built to be arranged. Therefore the power supply lines, the biases and common nodes run horizontally, while the input from the diode is computed vertically through the chip till it is hooked on a common line as output.

On the right side of the pixels the summadap circuit, the low power circuit and the threshold stage are laid out.

The bias generator is placed at the bottom of the chip. It is built to fit at a side of any chip. The design is very modular and is easy to adopt any requirements concerning bias currents. This part of the layout is likely to be used for other chips and therefore discussed in a special section.

On the left side of the pixels two stand-alone circuits are visible. The upper is the antibump threshold circuit and the lower the correlator circuit. The correlator circuit has to drive a beeper or a LED. To supply enough current the two transistors are made very short and wide. The whole correlator structure is embedded in a guard structure and separately powered, to protect the rest of the chip from its influenced. The stand-alone, adaptively biased photoreceptor circuit is placed in the upper left quarter of the chip.
Figure 3.1: The layout of the chip. The chip is framed by the pads. In the middle from the right to the left is the array of photodiodes placed. Underneath are the 30 pixels. On the right of the pixelarray the summadap circuit and the threshold stage are visible. The bias generator circuit occupies the lower side of the core. The stand-alone circuits are drawn near to the pads. The connections to the pads are chosen so to have as short distances as possible.
CHAPTER 3. THE ARCHITECTURE

To measure currents, a pFET and a nFET are added to the design in the upper right corner.

3.3 Bias Generator

The bias generator circuit has been designed by T. Delbrück for use on the physiology helper chip [6]. The circuits used for this project are nearly the same but the layout was newly designed for the AMS process in collaboration with Samuel Zahnd. It is made up of the masterbias module, the current divider network module and the nbias module (fig.(3.2)).

The masterbias circuit is designed long and thin in a rectangular shape. Half of the space is needed for the stabilizing capacitor on the right side, to achieve a capacitance of 34pF. The area with the transistors is covered with metal 2.

The outputs of the masterbias are two reference voltages GenNBias and GenNCasc. They are brought to the edge of the cell in the middle on both the upper and the lower side. Placed on the upper side of the masterbias are a ground and a Vdd wire and two wires connected to the node GenNBias and the node GenNCasc respectively so that they are available over the whole length. The vres node must be brought to a pad (see section(2.6)).

The current divider circuit [3] divides the master current by two each step. The resulting currents are fed into diode connected nFETs (W/L = 24μm/6μm) with their source hooked to ground. The output of the current divider network is the array of the gate voltages. They are hooked to wires running above the GenNBias and GenNCasc wires.

The nbiassource circuit is used different times. On the left side it is used to mirror the master current and source it as a pFET drain voltage to the current divider circuit. The nbiassource circuits right of the current divider circuit generate the needed bias currents. They can be placed modular besides each other on top of the gate voltage wires of the current divider network. The input node on the left side is hooked up to GenNCasc and the right input node to a reference voltage of the current divider network. Choosing the correct input generates a current according to the one in the current divider network. The nbiassource circuit sources this current out of a pFET. This current may now be divided or multiplied and fed into a required sized diode connected transistor.

The clear, modular architecture allows easy adaptation of the bias generator to different requirements.
Figure 3.2: The figure shows a part of the bias generator. For better resolution, the right side of the circuit is cut off and the circuit is turned ninety degrees. The bias generator circuit is composed of three circuits, the masterbias circuit, the nbias(source) circuit and the current divider circuit.
Chapter 4

The ultra low power motion detector

My work for this diploma thesis is concluded by sending out the test chip for fabrication. After the chip is back there is still a long way to go to a reliably working device and even longer if the device should reach product status.

First of all the chip has to be tested as a single piece. Secondly the device needs to be set up with the right optics and hooked up according to section (A.1). Thereafter it is hopefully possible to test the device in a real environment.

4.1 Measurements

The chip will be in a 64 pin package. It must be hooked up according to section (A.1). A lot of measurement points are available:

**Receptor** 4 output nodes to test if the receptor circuit works and to determine the visible field of the circuit, a node to measure or overdrive the bias current of the receptor circuit and a node to set the ground of the receptor circuit\(^1\).

**Bias generator** 13 pins are reserved to hook up and test the bias generator circuit.

**Threshold stage** 10 nodes are brought out for measurements and to hook up off-chip capacitors.

**Test antibump threshold** 5 nodes are brought out to test the antibump threshold circuit.

\(^1\)This node affects the DC photoreceptor output and may be used to modify the antibump dynamic range.
Biases The biases of all the circuits except the threshold circuits are brought out for measurements and to overdrive them if needed.

Transistors A nFET and pFET are placed separately on the chip, with the respective drain and gates hooked to pins. They are used for current measurements if only the gate voltages are available.

Correlator 4 pins are supplied to interface the chips.

Summadap To measure the summadap outputs and the summed antibump current 3 pads are used. An additional pin is reserved to clamp the clamp the ground of this circuit in order to move the output voltage.

The sum of the photo currents A feature to measure the summed photo currents via the stand-alone pFET.

The stand-alone photoreceptor To run the circuit entirely independent almost all its nodes are brought to pads.

All the bias currents can be measured via the stand-alone transistors. For example the antibump bias is determined by the gate voltage of a standard sized\(^2\) nFET whose source is tied to ground. The gate voltage, which is available on pin, has to be tied up to the gate of the stand-alone transistor. The source of the nFET is also tied to ground but the drain is brought to a pad. The current is measured by clamping the drain voltage.

The chip is designed for 3V but testing can go to 7 volts if long term reliability is not a concern.

4.2 The setup

The output nodes of the low power threshold circuits of two chips have to be tied to the inputs of the correlator circuit of one of the chips. This chip will be the one placed inside the room, the other will be the one in the hallway. The buzzer is tied to Vdd or even a higher voltage on one side and to the output of the correlator circuit on the other side. Both of the chips have to be tied to ground and Vdd. The assembling with off chip capacitances has to be done according to the schematics in the appendix.

Furthermore the chip needs to be set up with optics to focus the visible field onto the chip. To detect motion along the hallway a wide angle, cylindrical lens could be appropriate. The visible field of the chip is determined

\(^2\)The “standard” is defined in section (3.2).
by measurements on the output nodes of the receptor circuits placed on the right and on the left respectively.

4.3 The product appearance

The final product should look like a fancy high tech sticker. The two chips and the beeper have to be assembled directly on photo-voltaic cells included in the sticker. The cable has to be bendable and thin enough so that the gadget can be stuck directly to the door frame. Figure (4.1) shows how the device could appear on the gadget market.

4.4 Final remarks

It will be established not until the chip is tested if the goal of this thesis, to design an ultra low power motion detector, has been achieved by the work done so far. With the simulations and some calculations, I estimate that the chip will consume about \(10\mu W\) if it is on stand by \(^3\). This is ultra low power because the device would last on one set of two batteries longer then their shelf life\(^4\).

The power could be supplied by a solar cell under office lighting with the area of about \(5\text{cm}^2\) \(^5\).

Four months is a too short time to reach the state where you can present a reliably working CMOS device. The time passes too swiftly especially if

---

\(^3\) Stand by means if the buzzer and (or) the LED is not active.

\(^4\) A standard AA alkaline battery delivers about \(2Ah\) and has a shelf life below ten years.

\(^5\) Measurements: hallway \(\approx 100\text{mW/m}^2\), on the side where the sun is shining outside \(\approx 2\text{W/m}^2\), in the office (fluorescent) \(\approx 1\text{W/m}^2\). The efficiency of a solar cell is about 10% and it operates at about 1.5V. With this data the minimum photo voltaic area needed for two chips is calculated as, \(2 \times 2 \times 10\mu W \times \frac{1}{10\%} \times \frac{1\text{m}^2}{1\text{W}} = 4\text{cm}^2\). To power the buzzer as well a large storage capacitor can be used. The consequence is that the detector will then have a recovery time during which it would not buzz.
you get really fascinated by the work. I hope to come back to do some measurements and to set the device up somewhere in the INI.
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Appendix A

Schematics

A.1 Pins

The bonding diagram with the pin numbers will be provided by the manufacturer. Figure (A.1) shows the pad frame as a schematic. The corners are labeled. The according nodes are named and described in the tables (A.1) to (A.4).

A.2 Schematics of the circuits

Figures (A.2) to (A.9) show the detailed schematics of the circuits.

Figure (A.2) Schematic of the pads showing the pads used.

Figure (A.3) Schematic of the core. All the nodes are enumerated according to the tables (A.1) to (A.4) and the figure(A.1).

Figure (A.4) Schematic of the receptor circuit, the follower circuit and the antibump circuit.

Figure (A.5) Overview over the bias generator.

Figure (A.6) Schematics of the masterbias circuit, the biassource circuit, a circuit of the current divider network and the terminatory circuit of the current divider network.

Figure (A.7) Schematics of the lowPower circuit, the correlator circuit and the summadap circuit.

Figure (A.8) Schematics of the test antibump threshold circuit, the antibump threshold circuit, the low power threshold circuit and the delay circuit.
**Figure (A.9)** Schematic of the stand-alone adaptive biased receptor circuit.

The transistor lengths and widths are given in units of $\lambda = 0.4\mu m$. 
<table>
<thead>
<tr>
<th>#</th>
<th>name</th>
<th>function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gnd</td>
<td>ground</td>
</tr>
<tr>
<td>2</td>
<td>photocuRe</td>
<td>measure, current via stand-alone pFET</td>
</tr>
<tr>
<td>3</td>
<td>biasRe</td>
<td>measure or input, current via stand-along pFET</td>
</tr>
<tr>
<td>4</td>
<td>receptGndRe</td>
<td>input, voltage</td>
</tr>
<tr>
<td>5</td>
<td>outRe</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>6</td>
<td>follower Bias</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>7</td>
<td>folOut</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>8</td>
<td>testThresholdIn</td>
<td>input, voltage</td>
</tr>
<tr>
<td>9</td>
<td>testThresholdOutBias</td>
<td>input, current 1nA-1μA</td>
</tr>
<tr>
<td>10</td>
<td>testThresholdGndBias</td>
<td>input, current 1nA-1μA</td>
</tr>
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<td>11</td>
<td>testThresholdOut</td>
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<tr>
<td>12</td>
<td>testThresholdBumpOut</td>
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<td>correlatorGnd</td>
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<td>correlatorIn1</td>
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<td>15</td>
<td>correlatorIn2</td>
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<td>16</td>
<td>correlatorOut</td>
<td>output, current, hook to beeper or LED</td>
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Table A.1: pads 1 to 16

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<tr>
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<td>CVdd</td>
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<td>18</td>
<td>antibumpBias</td>
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<td>19</td>
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<td>21</td>
<td>16nA</td>
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<td>22</td>
<td>32nA</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>23</td>
<td>64nA</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>24</td>
<td>vres</td>
<td>off chip resistor, resistor to Gnd</td>
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<tr>
<td>25</td>
<td>biasGenNBias</td>
<td>measure, voltage</td>
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<tr>
<td>26</td>
<td>biasGenNCasc</td>
<td>measure, voltage</td>
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<tr>
<td>27</td>
<td>summadapVdd</td>
<td>measure, current with clamped voltage to Vdd</td>
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<tr>
<td>28</td>
<td>1nA via bias1M</td>
<td>measure, voltage</td>
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<td>29</td>
<td>128nA via bias1M</td>
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Table A.2: pads 17 to 32
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<td>PVdd</td>
<td>pad Vdd</td>
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<td>34</td>
<td>summadapGnd</td>
<td>input, clamp voltage (Gnd)</td>
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<td>out3</td>
<td>measure, voltage</td>
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<tr>
<td>36</td>
<td>out2</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>37</td>
<td>out1</td>
<td>measure, voltage</td>
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<td>38</td>
<td>delayOut3</td>
<td>measure, voltage and off chip capacitor</td>
</tr>
<tr>
<td>39</td>
<td>delayOut2</td>
<td>measure, voltage and off chip capacitor</td>
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<tr>
<td>40</td>
<td>delayOut1</td>
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<td>41</td>
<td>threshOut3</td>
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<td>42</td>
<td>threshOut2</td>
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<td>summadapOut</td>
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<td>44</td>
<td>threshOut1</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>45</td>
<td>summadapAd</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>46</td>
<td>biasDelay</td>
<td>inor, voltage</td>
</tr>
<tr>
<td>47</td>
<td>biasLowPower</td>
<td>inor, voltage</td>
</tr>
<tr>
<td>48</td>
<td>testNFetGate</td>
<td>input, voltage</td>
</tr>
</tbody>
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Table A.3: pads 33 to 48

<table>
<thead>
<tr>
<th>#</th>
<th>name</th>
<th>function</th>
</tr>
</thead>
<tbody>
<tr>
<td>49</td>
<td>FBias</td>
<td>follBias</td>
</tr>
<tr>
<td>50</td>
<td>testNFetDrain</td>
<td>measure, current with clamped voltage</td>
</tr>
<tr>
<td>51</td>
<td>testPFetGate</td>
<td>input, voltage</td>
</tr>
<tr>
<td>52</td>
<td>testPFetDrain</td>
<td>measure, current with clamped voltage</td>
</tr>
<tr>
<td>53</td>
<td>VuCurrent</td>
<td>inor, voltage</td>
</tr>
<tr>
<td>54</td>
<td>offChipCapLowPower</td>
<td>measure, voltage and off chip capacitor</td>
</tr>
<tr>
<td>55</td>
<td>receptOut4</td>
<td>measure, voltage</td>
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<tr>
<td>56</td>
<td>receptGnd</td>
<td>input, voltage</td>
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<td>57</td>
<td>photocurrent</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>58</td>
<td>adRe</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>59</td>
<td>receptOut3</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>60</td>
<td>receptOut2</td>
<td>measure, voltage</td>
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<tr>
<td>61</td>
<td>receptOut1</td>
<td>measure, voltage</td>
</tr>
<tr>
<td>62</td>
<td>gndRe</td>
<td>input, voltage</td>
</tr>
<tr>
<td>63</td>
<td>vddRe</td>
<td>input, voltage</td>
</tr>
<tr>
<td>64</td>
<td>offchipcapRe</td>
<td>off-chip capacitance to ground</td>
</tr>
</tbody>
</table>

Table A.4: pads 49 to 64
Figure A.1: The pin numbers
Figure A.2: schematics of pads
Figure A.3: schematics of core
Figure A.4: schematics of pixel
### Figure A.5: Schematics of Bias Generator

<table>
<thead>
<tr>
<th>PIXEL</th>
<th>ARRAY</th>
<th>SYM. THRESHOLD</th>
<th>DELAY</th>
<th>ASYM. THRES.</th>
<th>TEST</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Bias Follow 16nA" /></td>
<td><img src="image" alt="BiasLowPower 32nA" /></td>
<td><img src="image" alt="BiasThresGnd1 32nA" /></td>
<td><img src="image" alt="BiasDelay 1nA" /></td>
<td><img src="image" alt="BiasThresGndEnd 32nA" /></td>
<td><img src="image" alt="1nA via bias1m" /></td>
</tr>
<tr>
<td><img src="image" alt="BiasBump 32nA" /></td>
<td><img src="image" alt="BiasSummadap 3*128nA" /></td>
<td><img src="image" alt="BiasThresGnd2 32nA" /></td>
<td><img src="image" alt="BiasThresOut2 16/3nA" /></td>
<td><img src="image" alt="BiasThresOutEnd 16nA" /></td>
<td><img src="image" alt="128nA via bias1n" /></td>
</tr>
<tr>
<td><img src="image" alt="BiasThresGnd3 32nA" /></td>
<td><img src="image" alt="BiasThresOut 8nA" /></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure A.6: schematics2 of bias generator
Figure A.7: schematics of lowPower, correlator, summadap
Figure A.8: schematics of threshold stage
Figure A.9: schematics stand-alone receptor
Appendix B

Netlist of the core

* SPICE netlist written by S-Edit Win32 7.02
* Written on Mar 15, 2002 at 13:53:52

.SUBCKT Inorpad pad Gnd
X1 pad padbond
M2_3_1 pad Gnd Gnd Gnd NMOS1 L=2 \( W=250 \) \( AD=(60\times3)+36' \) PD='60+6+6' AS=(60\times3)+36' PS='60+6+6' M=1
* S-Edit ID pad, only grounded gate ESD protection
* Designed by: tobi Feb 6, 2002 12:01:13
* Schematic generated by S-Edit
* from file \%Zener\patrick\diplomwork\edit\officeguardlvs / module Inorpad / page Page0
.END

.SUBCKT barepad pad
X1 pad padbond
* S-Edit 2D motion chip AMS 0.8um
* Designed by: alan stocker Feb 15, 2002 08:41:57
* Schematic generated by S-Edit
* from file \%Zener\patrick\diplomwork\edit\officeguardlvs / module barepad / page Page0
.END

* No Ports in cell: .pageID
* End of module with no ports: .pageID

.SUBCKT biassource nbias ncasc out Gnd Vdd
M3_5 nmid nbias Gnd Gnd NMOS1 L=15 \( W=60 \) AD=(60\times3)+36' PD='60+6+6' AS=(60\times3)+36' PS='60+6+6' M=1
M3_10 N4 ncasc nmid Gnd NMOS1 L=15 \( W=60 \) AD=(60\times3)+36' PD='60+6+6' AS=(60\times3)+36' PS='60+6+6' M=1
M3_4 N7 pmid Vdd Vdd PMOS1 L=15 \( W=60 \) AD=(60\times3)+36' PD='60+6+6' AS=(60\times3)+36' PS='60+6+6' M=1
M3_5 pmid pmid Vdd Vdd PMOS1 L=15 \( W=60 \) AD=(60\times3)+36' PD='60+6+6' AS=(60\times3)+36' PS='60+6+6' M=1
M4_1 N4 N4 nmid pmid PMOS1 L=15 \( W=60 \) AD=(60\times3)+36' PD='60+6+6' AS=(60\times3)+36' PS='60+6+6' M=1
M4_2 out N4 N7 pmid PMOS1 L=15 \( W=60 \) AD=(60\times3)+36' PD='60+6+6' AS=(60\times3)+36' PS='60+6+6' M=1
.END

.SUBCKT biasnim in out BiasGenNCasc Gnd Vdd
Xbiassource_1 in BiasGenNCasc out Gnd Vdd biassource
M3_1 Gnd out out Gnd NMOS1 L=15 \( W=15 \) AD=(15\times3)+36' PD='15+6+6' AS=(15\times3)+36' PS='15+6+6' M=1
.EEND
.SUBCKT bias3d in out BiasGenNCasc Gnd Vdd
Xbiassource_1 in BiasGenNCasc out Gnd Vdd biassource
MB3_1 Gnd out Gnd NMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
MB3_2 Gnd out Gnd NMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
MB3_3 Gnd out Gnd NMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
.ENDS

.SUBCKT bias3n in out BiasGenNCasc Gnd Vdd
Xbiassource_4 in BiasGenNCasc N=14 Gnd Vdd biassource
MB3_6 Gnd N=14 N=14 Gnd NMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
MB3_9 N=14 Gnd Gnd NMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
MB3_11 N=14 Gnd Gnd NMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
MB3_17 out Gnd Gnd NMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
MP3_1 Vdd N=9 N=9 Vdd PMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
MP3_2 out N=9 Vdd Vdd PMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
.ENDS

.SUBCKT masterbias vres BiasGenNBias BiasGenNCasc Gnd Vdd
C1 Gnd kickgate 250f
C2 prirrorin Vdd 250f
C3 prirrorin BiasGenNCasc 3p
MB3_1 BiasGenNCasc BiasGenNCasc BiasGenNBias Gnd NMOS L=15 W=60 AD='(60x3)+36' PD='60+6+6' AS='(60x3)+36' PS='60+6+6' N=1
MB3_2 nmirorout BiasGenNCasc prirrorin Gnd NMOS L=15 W=60 AD='(60x3)+36' PD='60+6+6' AS='(60x3)+36' PS='60+6+6' N=1
Mbias BiasGenNBias BiasGenNCasc Gnd NMOS L=15 W=60 AD='(60x3)+36' PD='60+6+6' AS='(60x3)+36' PS='60+6+6' N=1
Mares nmirorout BiasGenNBias vres Gnd NMOS L=15 W=60 AD='(60x3)+36' PD='60+6+6' AS='(60x3)+36' PS='60+6+6' N=27
MP3_1 prirrorin prirrorin Vdd Vdd PMOS L=60 W=30 AD='(30x3)+36' PD='30+6+6' AS='(30x3)+36' PS='30+6+6' N=1
MP3_2 BiasGenNCasc prirrorin Vdd PMOS L=60 W=30 AD='(30x3)+36' PD='30+6+6' AS='(30x3)+36' PS='30+6+6' N=1
MP3_3 BiasGenNCasc kickgate Vdd PMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
MP3_4 kickgate prirrorin Vdd PMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
.ENDS

.SUBCKT nbiassourceMeasure in out BiasGenNCasc Gnd Vdd
Xbiassource_1 in BiasGenNCasc N=5 Gnd Vdd biassource
MB3_1 out N=5 N=5 Gnd NMOS L=15 W=15 AD='(15x3)+36' PD='15+6+6' AS='(15x3)+36' PS='15+6+6' N=1
.ENDS

.SUBCKT resetcompartment left out right BiasGenNBias Gnd Vdd
MB3_1 out Gnd Gnd NMOS L=15 W=60 AD='(60x3)+36' PD='60+6+6' AS='(60x3)+36' PS='60+6+6' N=1
MB3_1 right BiasGenNBias left Vdd PMOS L=15 W=60 AD='(60x3)+36' PD='60+6+6'
APPENDIX B. NETLIST OF THE CORE

```
AS='(60*3)+36' PS='60+6+6' N=1
M3_2 .right BiasGenNBias left Vdd PMOS1 L=15 W=60 AD='(60*3)+36' PD='60+6+6'
AS='(60*3)+36' PS='60+6+6' N=1
M3_4 .out BiasGenNBias right Vdd PMOS1 L=15 W=60 AD='(60*3)+36' PD='60+6+6'
AS='(60*3)+36' PS='60+6+6' N=1
.ENDS

.SUBCKT resnetend left out BiasGenNBias Gnd Vdd
M3_1 Gnd out out Gnd NMOS1 L=15 W=60 AD='(60*3)+36' PD='60+6+6' AS='(60*3)+36'
PS='60+6+6' N=1
M3_1 N5 BiasGenNBias left Vdd PMOS1 L=15 W=60 AD='(60*3)+36' PD='60+6+6' AS='(60*3)+36'
PS='60+6+6' N=1
M3_3 .out BiasGenNBias N5 Vdd PMOS1 L=15 W=60 AD='(60*3)+36' PD='60+6+6' AS='(60*3)+36'
PS='60+6+6' N=1
.ENDS

.SUBCKT biasgenlvvs vres 128mA via_biaasn1m inA via_biaasn1m bias16m biasm bias2m
+ bias23m bias3m bias6 sn biasBmp biasDaly biasFollw BiasGenNBias
+ BiasGenNcasc biaslowsPower biasSummadap biasThreeGnd1 biasThreeGnd2 biasThreeGnd3
+ biasThreeGnd3t biasThreeOut2 biasThreeOut3 biasThreeOut4t Gnd Vdd
Xbiasim4_1 biasf0n biasFollw BiasGenNcasc Gnd Vdd biasim1
Xbiasim4_2 bias32n biasBmp BiasGenNcasc Gnd Vdd biasim1
Xbiasim4_3 bias8n biasThreeOutEnd BiasGenNcasc Gnd Vdd biasim1
Xbiasim4_10 biasin biasDelay BiasGenNcasc Gnd Vdd biasim1
Xbiasim4_1 bias32n biasThreeOut2 BiasGenNcasc Gnd Vdd bias3m
Xbiasim4_1 BiasGenNBias biasSummadap BiasGenNcasc Gnd Vdd bias3m
Xbiassource 5 BiasGenNBias BiasGenNcasc N9 Gnd Vdd biassource
Anmasterbias_1 vres BiasGenNBias BiasGenNcasc Gnd Vdd masterbias
XbiassourceMeasure_1 biasm inA via_biaasn1m BiasGenNcasc Gnd Vdd
+ nbiassourceMeasure
XbiassourceMeasure_2 BiasGenNBias 128mA via_biaasn1m BiasGenNcasc Gnd Vdd
+ nbiassourceMeasure
Xresnetcompartmant_1 N9 bias6n N1G BiasGenNBias Gnd Vdd resnetcompartmant
Xresnetcompartmant_2 N1G bias32n N18 BiasGenNBIasc Gnd Vdd resnetcompartmant
Xresnetcompartmant_3 N18 bias16n N17 BiasGenNBias Gnd Vdd resnetcompartmant
Xresnetcompartmant_4 N17 bias6n N16 BiasGenNBias Gnd Vdd resnetcompartmant
Xresnetcompartmant_5 N16 bias3n N14 BiasGenNBIasc Gnd Vdd resnetcompartmant
Xresnetcompartmant_6 N14 bias16n BiasGenNBIasc Gnd Vdd resnetcompartmant
Xresnetend_1 N14 biasm BiasGenNBIasc Gnd Vdd resnetend
.ENDS

.SUBCKT correlator Cnd in1 in2 out Gnd Vdd
M3_1 N1 in2 Gnd Gnd NMOS1 L=2 W=101 AD='(101+3)+36' PD='101+6+6' AS='(101+3)+36'
PS='101+6+6' N=1
M3_2 out in1 N1 Gnd NMOS1 L=2 W=101 AD='(101+3)+36' PD='101+6+6' AS='(101+3)+36'
PS='101+6+6' N=1
.ENDS

.SUBCKT delay in out biasDelay Gnd Vdd
M3_1 Vdd in out Gnd NMOS1 L=15 W=60 AD='(60*3)+36' PD='60+6+6' AS='(60*3)+36'
PS='60+6+6' N=3
M3_2 out biasDelay Gnd Gnd NMOS1 L=90 W=15 AD='(15*3)+36' PD='15+6+6' AS='(15*3)+36'
PS='15+6+6' N=1
.ENDS

* No Ports in cell: diodeP
* End of module with no ports: diodeP

.SUBCKT lowPowerRe bias cap iin vout Gnd Vdd
Mbias Gnd bias cap Gnd NMOS1 L=15 W=15 AD='(15*3)+36' PD='15+6+6' AS='(15*3)+36'
PS='15+6+6' N=1
M3_2 Gnd cap vout Gnd NMOS1 L=15 W=15 AD='(15*3)+36' PD='15+6+6' AS='(15*3)+36'
```
APPENDIX B. NETLIST OF THE CORE

PS=15+6+6' M=1
Mfb idiode center in Gnd NMOS1 L=15 W=15 AD='(45+3)+36' PD=45+6+6' AS='(45+3)+36'
PS=45+6+6' M=1
Mpmp out bias Vdd Vdd PMOS1 L=15 W=15 AD='(15+3)+36' PD='15+6+6' AS='(15+3)+36'
PS='15+6+6' M=1
.ENDS

.SUBCkt pixel biasRecept follOut ibg in out receptorGnd receptorOut biasBump
+ biasTlow Gnd Vdd
Xfollow_1 receptorOut follOut biasTlow Gnd Vdd follow
Xbias_1 receptorOut follOut out biasBump Gnd Vdd nump
Xrecep_1 biasRecept ibg in receptorOut receptorGnd Gnd Vdd receptor
.ENDS

.SUBCkt receptor adelRe bias idiole in out Gnd Gnd Vdd
Md adelRe adelRe out out PMOS1 L=26 W=15 AD='(15+3)+36' PD='15+6+6' AS='(15+3)+36'
PS='15+6+6' M=1
Cl adelRe Gnd 3.72p
C2 adelRe out 10.1f
Mpmp out in out Gnd Gnd NMOS1 L=15 W=15 AD='(15+3)+36' PD='15+6+6' AS='(15+3)+36'
PS='15+6+6' M=1
Mfb idiode adelRe in Gnd NMOS1 L=15 W=45 AD='(45+3)+36' PD='45+6+6' AS='(45+3)+36'
PS='45+6+6' M=1
Mpmp out bias Vdd Vdd PMOS1 L=15 W=15 AD='(15+3)+36' PD='15+6+6' AS='(15+3)+36'
PS='15+6+6' M=1
.ENDS

.SUBCkt landolt_300 in out Gnd Vdd
.param AV=30
.param AL=15
.param MH=15
.param BL=15
Mb1 s1 in n2 Gnd NMOS1 L=AL W=AV AD='(AV+3)+36' PD='AV+6+6' AS='(AV+3)+36' PS='AV+6+6' M=1
Mb2 s2 in n3 Gnd NMOS1 L=AL W=AV AD='(AV+3)+36' PD='AV+6+6' AS='(AV+3)+36' PS='AV+6+6' M=1
Mb3 s3 in n4 Gnd NMOS1 L=AL W=AV AD='(AV+3)+36' PD='AV+6+6' AS='(AV+3)+36' PS='AV+6+6' M=1
Mb4 s4 in n5 Gnd NMOS1 L=AL W=AV AD='(AV+3)+36' PD='AV+6+6' AS='(AV+3)+36' PS='AV+6+6' M=1
Mb5 s5 in n6 Gnd NMOS1 L=AL W=AV AD='(AV+3)+36' PD='AV+6+6' AS='(AV+3)+36' PS='AV+6+6' M=1
Mb6 s6 in n7 Gnd NMOS1 L=AL W=AV AD='(AV+3)+36' PD='AV+6+6' AS='(AV+3)+36' PS='AV+6+6' M=1
Mb7 s7 in n8 Gnd NMOS1 L=AL W=AV AD='(AV+3)+36' PD='AV+6+6' AS='(AV+3)+36' PS='AV+6+6' M=1
Mb8 s8 in Gnd Gnd NMOS1 L=AL W=AV AD='(AV+3)+36' PD='AV+6+6' AS='(AV+3)+36' PS='AV+6+6' M=1
M10 in n1 Gnd NMOS1 L=BL W=EN AD='(EN+3)+36' PD='BN+6+6' AS='(EN+3)+36' PS='BN+6+6' M=1
M11 Vdd in s1 Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
M12 Vdd in s2 Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
M13 out in s3 Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
M14 out in s4 Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
M15 Vdd in s5 Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
M16 out in s6 Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
M17 Vdd in s7 Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
M18 Vdd in s8 Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
M19 out in Gnd Gnd NMOS1 L=BL W=VW AD='(BV+3)+36' PD='BN+6+6' AS='(BV+3)+36' PS='BN+6+6' M=1
.ENDS

.SUBCkt standalone_recept in out Gnd Vdd
Xlandolt_300_i NG N1 Gnd Vdd landolt_300
MP3_1 in in Vdd Vdd PMOS1 L=15 W=15 AD='(15+3)+36' PD='15+6+6' AS='(15+3)+36' PS='15+6+6'
M=1
MP3_2 N6 in Vdd Vdd PMOS1 L=15 W=15 AD='(15+3)+36' PD='15+6+6' AS='(15+3)+36' PS='15+6+6'
M=1
MP3_3 N1 N1 Vdd Vdd PMOS1 L=15 W=15 AD='(15+3)+36' PD='15+6+6' AS='(15+3)+36' PS='15+6+6'
M=1
Mpmp out N1 Vdd Vdd PMOS1 L=15 W=15 AD='(15+3)+36' PD='15+6+6' AS='(15+3)+36' PS='15+6+6'
M=1
.ENDS

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APPENDIX B. NETLIST OF THE CORE

.ENDS

.SUBCKT summadap ad in out sGnd sVdd biasSummadap Gnd Vdd
Nad ad ad out pmos1 L=25 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
Cl ad Gnd 5.9p
C2 ad out 10f
MB3_1 Gnd biasSummadap N19 Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
Mnump out in Gnd Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
Mfb sVdd ad in Gnd NMOS1 L=15 W=15 AD=’(45x3)+36’ PD=’45+6+6’ AS=’(45x3)+36’ PS=’45+6+6’ N=1
MF3_1 Vdd N19 N19 Vdd PMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
Mnump out N19 Vdd Vdd PMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
.ENDS

.SUBCKT testNFet drain vg Gnd
NF3_1 drain vg Gnd Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
-ENDS

.SUBCKT testPFet drain vg Vdd
MF3_1 drain vg Vdd Vdd PMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
.ENDS

.SUBCKT testThreshold bumpOut in out th thGnd thOut Gnd Vdd
MF3_1 N3 in N1 Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_2 out thOut Gnd Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_3 Gnd thOut bumpOut Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_4 N1 th N3 Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_5 N1 thGnd Gnd Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_6 thOut thOut Gnd Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_7 thGnd thGnd Gnd Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_8 N1 Vdd bumpOut Vdd PMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_9 N3 Vdd PMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MF3_10 N3 Vdd PMOS1 L=15 W=30 AD=’(30x3)+36’ PD=’30+6+6’ AS=’(30x3)+36’ PS=’30+6+6’ N=1
MF3_11 N3 Vdd bumpOut Vdd PMOS1 L=15 W=30 AD=’(30x3)+36’ PD=’30+6+6’ AS=’(30x3)+36’ PS=’30+6+6’ N=1
MF3_12 N3 Vdd PMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
.ENDS

.SUBCKT threshold_asym in out th biasBump biasFollow Gnd Vdd
MB3_1 N3 in N1 Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MB3_2 out biasFollow Gnd Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MB3_3 Gnd biasFollow N6 Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MB3_4 N1 th N3 Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
MB3_5 N1 biasBump Gnd Gnd NMOS1 L=15 W=15 AD=’(15x3)+36’ PD=’15+6+6’ AS=’(15x3)+36’ PS=’15+6+6’ N=1
.ENDS
APPENDIX B. NETLIST OF THE CORE

55

MP3_1 out N6 Vdd Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_2 Vdd N3 N3 Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_4 Vdd N8 N6 Vdd PMOS1 L=15 W=30 AD=('30*3)+36' PD='30+6+6' AS='(30*3)+36' PS='30+6+6'
M=1
MP3_5 N8 N8 Vdd Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
.ENDS

..SUBCKT threshold_sym3 in1 in2 out thQnd thOut Gnd Vdd
MP3_1 N15 in1 N1 Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_2 out thOut Gnd Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_3 Gnd thOut N2 Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_4 N1 in2 N6 Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_5 N1 thGnd Gnd Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_1 out N2 Vdd Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_2 Vdd N15 N15 Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_3 N19 N8 Vdd Vdd PMOS1 L=15 W=30 AD=('30*3)+36' PD='30+6+6' AS='(30*3)+36' PS='30+6+6'
M=1
MP3_4 N19 N15 N2 Vdd PMOS1 L=15 W=30 AD=('30*3)+36' PD='30+6+6' AS='(30*3)+36' PS='30+6+6'
M=1
MP3_5 N8 N8 Vdd Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
.ENDS

..SUBCKT threshold_sym in1 in2 out thQnd thOut Gnd Vdd
MP3_1 N4 in1 N1 Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_2 out thOut Gnd Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_3 Gnd thOut N6 Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_4 N1 in2 N2 Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_5 N1 thGnd Gnd Gnd NMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_1 out N6 Vdd Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_2 Vdd N4 N4 Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
MP3_3 N3 N2 Vdd Vdd PMOS1 L=15 W=30 AD=('30*3)+36' PD='30+6+6' AS='(30*3)+36' PS='30+6+6'
M=1
MP3_4 N3 N4 N6 Vdd PMOS1 L=15 W=30 AD=('30*3)+36' PD='30+6+6' AS='(30*3)+36' PS='30+6+6'
M=1
MP3_5 N2 N2 Vdd PMOS1 L=15 W=15 AD=('15*3)+36' PD='15+6+6' AS='(15*3)+36' PS='15+6+6'
M=1
.ENDS

..SUBCKT corePlvs 128mA_via_biasim1 inA via_biasim1 adRe bias16mA bias16mA bias2n + bias2mA bias4mA bias6mA bias8mA bias12mA biasDelay biasFollow BiasGenNBin + BiasGenNInc biasRe correlateGnd correlateIn1 correlateIn2 correlateOut + delayOut1 delayOut2 delayOut3 follOut offChipOnLowPower offchipcapRe out1 out2 + out3 outRe photocoule photocurrent receptorGnd receptorGndRe receptorOut1 receptorOut2 + receptorOut3 receptorOut4 summadapAd summadapGnd summadapOut summadapVdd
APPENDIX B. NETLIST OF THE CORE

+ testNFetDRAIN  testNFetGATE  testNFetDRAIN  testNFetGATE  testThresholdDumpOut
+ testThresholdQNDBias  testThresholdIn  testThresholdOut  testThresholdOutBias
+ threshold threeOut1 threeOut2 threeOut3 vreV Current  biasLowPower  biasSummadap
+ biasThreeGnd1  biasThreeGnd2  biasThreeGnd3  biasThreeGnd4  biasThreeGndEnd  biasThreeOut2
+ biasThreeOut3  biasThreeOutEnd  Gnd Vdd
XbiasGenNsVr1 vre1 128mA via_biasN1m 1mA via_biasm1n  bias16m  bias16n
+ bias20n  bias84n  bias8m  bias8n  biasBump  biasDelay  biasFollow  BiasGenNiBias
+ BiasGenXCan  biasLowPower  biasSummadap  biasThreeGnd1  biasThreeGnd2  biasThreeGnd3
+ biasThreeGndEnd  biasThreeOut2  biasThreeOut3  biasThreeOutEnd  Gnd Vdd  biasGenUlVs
Xcorrelator_1  correlatorIn1  correlatorIn2  correlatorOut  Gnd Vdd
+ correlator
Xdelay_1 threeOut3  delayOut3  biasDelay  Gnd Vdd  delay
Xdelay_2 threeOut2  delayOut2  biasDelay  Gnd Vdd  delay
Xdelay_3 threeOut1  delayOut1  biasDelay  Gnd Vdd  delay
XlowpowerRe_1 testThresholdOutBiaS  offChipCapRe  N119  biasRe  Gnd Vdd  lowPowerRe
XlowPower_1 offChipCapLowPower  photocurrent  VCurrent  biasFollow  Gnd Vdd
+ lowPower
Xpixel_1 VCurrent  follOut  photocurrent  in1  N111  recepGnd  recepOut1  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_2 VCurrent  follOut  photocurrent  in2  N111  recepGnd  N26  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_3 VCurrent  follOut  photocurrent  in3  N111  recepGnd  N25  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_4 VCurrent  follOut  photocurrent  in4  N111  recepGnd  N32  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_5 VCurrent  follOut  photocurrent  in5  N111  recepGnd  N35  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_6 VCurrent  follOut  photocurrent  in6  N111  recepGnd  N38  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_7 VCurrent  follOut  photocurrent  in7  N111  recepGnd  N41  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_8 VCurrent  follOut  photocurrent  in8  N111  recepGnd  N44  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_9 VCurrent  follOut  photocurrent  in9  N111  recepGnd  N47  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_10 VCurrent  follOut  photocurrent  in10  N111  recepGnd  N50  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_11 VCurrent  follOut  photocurrent  in11  N111  recepGnd  N53  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_12 VCurrent  follOut  photocurrent  in12  N111  recepGnd  N56  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_13 VCurrent  follOut  photocurrent  in13  N111  recepGnd  N59  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_14 VCurrent  follOut  photocurrent  in14  N111  recepGnd  N62  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_15 VCurrent  follOut  photocurrent  in15  N111  recepGnd  recepOut2  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_16 VCurrent  follOut  photocurrent  in16  N111  recepGnd  recepOut3  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_17 VCurrent  follOut  photocurrent  in17  N111  recepGnd  N71  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_18 VCurrent  follOut  photocurrent  in18  N111  recepGnd  N74  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_19 VCurrent  follOut  photocurrent  in19  N111  recepGnd  N77  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_20 VCurrent  follOut  photocurrent  in20  N111  recepGnd  N80  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_21 VCurrent  follOut  photocurrent  in21  N111  recepGnd  N83  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_22 VCurrent  follOut  photocurrent  in22  N111  recepGnd  N86  biasBump
+ biasFollow  Gnd Vdd  pixel
Xpixel_23 VCurrent  follOut  photocurrent  in23  N111  recepGnd  N89  biasBump
APPENDIX B. NETLIST OF THE CORE

+ biasFollow Gnd Vdd pixel
  Xpixel_24 VuCurrent f01Out photocurrent in24 N111 recept.Gnd N92 biasBump
+ biasFollow Gnd Vdd pixel
  Xpixel_25 VuCurrent f01Out photocurrent in25 N111 recept.Gnd N96 biasBump
+ biasFollow Gnd Vdd pixel
  Xpixel_26 VuCurrent f01Out photocurrent in26 N111 recept.Gnd N98 biasBump
+ biasFollow Gnd Vdd pixel
  Xpixel_27 VuCurrent f01Out photocurrent in27 N111 recept.Gnd N101 biasBump
+ biasFollow Gnd Vdd pixel
  Xpixel_28 VuCurrent f01Out photocurrent in28 N111 recept.Gnd N104 biasBump
+ biasFollow Gnd Vdd pixel
  Xpixel_29 VuCurrent f01Out photocurrent in29 N111 recept.Gnd N107 biasBump
+ biasFollow Gnd Vdd pixel
  Xpixel_30 VuCurrent f01Out photocurrent in30 N111 recept.Gnd receptOut4 biasBump
+ biasFollow Gnd Vdd pixel
XreceptRe_1 adRe biasRe photocupRe N115 outRe receptGndRe Gnd Vdd receptRe
XreceptRe_1 pouchE N119 Gnd Vdd standalone_recept
Xsummadap_1 summadapAd N111 summadapOut summadapGnd summadapVdd biasSummadap Gnd + Vdd summadap
4xtestNfet_1 testNfetDrain testNfetGate Gnd testNfet
4xtestPfet_1 testPfetDrain testPfetGate Vdd testPfet
4xtestThreshold_1 testThresholdBumpOut testThresholdIn testThresholdOut threshold
+ testThresholdOutBias testThresholdOutBias Gnd Vdd testThreshold
Xthreshold_asym_1 delayOut3 out3 threshold biasBump biasFollow Gnd Vdd + threshold_asym
Xthreshold_asym_2 delayOut2 out2 threshold biasBump biasFollow Gnd Vdd + threshold_asym
Xthreshold_asym_3 delayOut1 out1 threshold biasBump biasFollow Gnd Vdd + threshold_asym
Xthreshold_sym_1 summadapAd summadapOut thresOut3 biasBump biasFollow Gnd Vdd + threshold_sym3
Xthreshold_sym_2 summadapAd summadapOut thresOut2 biasBump biasThresOut2 Gnd Vdd + threshold_sym
Xthreshold_sym_3 summadapAd summadapOut thresOut1 biasBump biasThresOutEnd Gnd + Vdd threshold_sym
.ENDS

* No Ports in cell: PageID2
* End of module with no ports: PageID2

.SUBCKT FollowerPad in pad Gnd
X1 pad padbond
N9_3_1 in Gnd Gnd Gnd NMS1 L=2 W=250 AD='(250+3)+36' PD='250+6+6' AS='(250+3)+36'
+ PS='250+6+6' M=1
R2 pad in 4152
.ENDS

.SUBCKT inpad in pad Gnd
X1 pad padbond
N9_3_1 in Gnd Gnd Gnd NMS1 L=2 W=250 AD='(250+3)+36' PD='250+6+6' AS='(250+3)+36'
+ PS='250+6+6' M=1
R2 pad in 1500
.ENDS

.SUBCKT outpad-notermLowPower out pad Gnd PadVdd
X1 pad padbond
N93_1 pad N5 Gnd Gnd NMS1 L=2 W=40 AD='(40+3)+36' PD='40+6+6' AS='(40+3)+36' PS='40+6+6'
+ M=1
N93_2 N5 out Gnd Gnd NMS1 L=2 W=40 AD='(40+3)+36' PD='40+6+6' AS='(40+3)+36' PS='40+6+6'
+ M=1
N94_1 pad N5 PadVdd PadVdd PMOS1 L=2 W=40 AD='(40+3)+36' PD='40+6+6' AS='(40+3)+36'
+ PS='40+6+6' M=1
`#ENDS

.SUBCKT widepad pad wide FollBias Gnd PadVdd

X1 pad padbond

M13_1 N42 pad N5 Gnd NMOS1 L=12.5 W=12.5 $AD=(12.5\times3)+36$ $PD=12.5+6+6$ $AS=(12.5\times3)+36$

$PS=12.5+6+6 \ M=1$

M13_2 noutgate wide N5 Gnd NMOS1 L=12.5 W=12.5 $AD=(12.5\times3)+36$ $PD=12.5+6+6$

$AS=(12.5\times3)+36$ $PS=12.5+6+6 \ M=1$

M13_3 N5 FollBias Gnd Gnd NMOS1 L=12.5 W=12.5 $AD=(12.5\times3)+36$ $PD=12.5+6+6$

$AS=(12.5\times3)+36$ $PS=12.5+6+6 \ M=1$

M13_4 N10 N10 Gnd Gnd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$ $AS=(23.5\times3)+36$

$PS=23.5+6+6 \ M=1$

M13_5 noutgate N10 Gnd Gnd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$ $AS=(23.5\times3)+36$

$PS=23.5+6+6 \ M=1$

M13_6 pbias FollBias Gnd Gnd NMOS1 L=12.5 W=12.5 $AD=(12.5\times3)+36$ $PD=12.5+6+6$

$AS=(12.5\times3)+36$ $PS=12.5+6+6 \ M=1$

M13_7 noutgate noutgate Gnd Gnd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(23.5\times3)+36$ $PS=23.5+6+6 \ M=1$

M14_2 noutgate noutgate Gnd Gnd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(23.5\times3)+36$ $PS=23.5+6+6 \ M=1$

M14_3 pad noutgate Gnd Gnd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(54.5\times3)+36$ $PS=54.5+6+6 \ M=8$

M14_10 pad noutgate Gnd Gnd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(54.5\times3)+36$ $PS=54.5+6+6 \ M=8$

M14_1 pbias pbias PadVdd PadVdd NMOS1 L=6 W=54.5 $AD=(54.5\times3)+36$ $PD=54.5+6+6$

$AS=(54.5\times3)+36$ $PS=54.5+6+6 \ M=8$

M14_2 N37 pbiasPadVdd PadVdd NMOS1 L=12.5 W=12.5 $AD=(12.5\times3)+36$ $PD=12.5+6+6$

$AS=(12.5\times3)+36$ $PS=12.5+6+6 \ M=1$

M14_4 N37 pad noutgate N37 PadVdd NMOS1 L=12.5 W=12.5 $AD=(12.5\times3)+36$ $PD=12.5+6+6$

$AS=(12.5\times3)+36$ $PS=12.5+6+6 \ M=1$

M14_10 pad N37 PadVdd NMOS1 L=12.5 W=12.5 $AD=(12.5\times3)+36$ $PD=12.5+6+6$

$AS=(12.5\times3)+36$ $PS=12.5+6+6 \ M=1$

M14_1 N42 N42 PadVdd PadVdd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(23.5\times3)+36$ $PS=23.5+6+6 \ M=1$

M14_6 noutgate N42 PadVdd PadVdd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(23.5\times3)+36$ $PS=23.5+6+6 \ M=1$

M14_7 pbias pbias PadVdd PadVdd NMOS1 L=12.5 W=12.5 $AD=(12.5\times3)+36$ $PD=12.5+6+6$

$AS=(12.5\times3)+36$ $PS=12.5+6+6 \ M=1$

M14_8 noutgate noutgate PadVdd PadVdd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(23.5\times3)+36$ $PS=23.5+6+6 \ M=1$

M14_9 noutgate noutgate PadVdd PadVdd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(23.5\times3)+36$ $PS=23.5+6+6 \ M=1$

M14_10 noutgate noutgate PadVdd PadVdd NMOS1 L=6 W=23.5 $AD=(23.5\times3)+36$ $PD=23.5+6+6$

$AS=(23.5\times3)+36$ $PS=23.5+6+6 \ M=1$

#ENDS

* Main circuit: chipFlv

Xbarepad_20 Gnd barepad

Xbarepad_21 Vdd barepad

Xbarepad_22 PadVdd barepad

XcoreFlv_1 N20 N18 N10 N19 N3 N7 N27 N11 N23 N15 N8 N78 N76 N12 N14 N4 Gnd N74


N62 N23 N60 N16 N30 N28 N6 N32 N66 N31 N42 N64 N36 N40 N52 N50 N48 N46 N10 N34

biasLowPower biasSummedap biasThreeGnd1 biasThreeGnd2 biasThreeGnd3

biasThreeGndEnd biasThreeOut2 biasThreeOut3 biasThreeOutEnd Gnd Vdd coreFlv

XFollowerpad_2 FollBias N82 Gnd Followerpad

Xiorpad_1 N44 Gnd Inorpad

Xiorpad_2 Gnd Gnd Inorpad

Xiorpad_3 N42 Gnd Inorpad

Xiorpad_4 N40 Gnd Inorpad
APPENDIX B. NETLIST OF THE CORE

Xnorpad_5 N38 Gnd Inorpad
Xnorpad_6 N36 Gnd Inorpad
Xnorpad_7 N34 Gnd Inorpad
Xnorpad_8 N32 Gnd Inorpad
Xnorpad_9 N30 Gnd Inorpad
Xnorpad_10 N28 Gnd Inorpad
Xnorpad_11 N26 Gnd Inorpad
Xnorpad_12 N24 Gnd Inorpad
Xnorpad_13 N22 Gnd Inorpad
Xnorpad_14 N20 Gnd Inorpad
Xnorpad_15 N18 Gnd Inorpad
Xnorpad_16 N16 Gnd Inorpad
Xnorpad_17 N14 Gnd Inorpad
Xnorpad_18 N12 Gnd Inorpad
Xnorpad_19 N10 Gnd Inorpad
Xnorpad_20 N8 Gnd Inorpad
Xnorpad_21 N6 Gnd Inorpad
Xnorpad_22 N4 Gnd Inorpad
Xnorpad_23 N2 Gnd Inorpad
Xnorpad_24 Gnd Inorpad
Xnorpad_25 N30 Gnd Inorpad
Xnorpad_26 Vdd Gnd Inorpad
Xnorpad_27 N30 Gnd Inorpad
Xpad_1 N54 N34 Gnd inpad
Xpad_2 N74 N36 Gnd inpad
Xpad_3 N72 N38 Gnd inpad
Xpad_4 N70 N39 Gnd inpad
Xpad_5 N78 N37 Gnd inpad
Xpad_6 N76 N35 Gnd inpad
Xpad_7 N76 N31 Gnd inpad
Xpad_8 N76 N79 Gnd inpad
Xpad_9 N76 N79 Gnd inpad

Xoutpad-notermLowPower_1 N64 N75 Gnd PadVdd outpad-notermLowPower
Xoutpad-notermLowPower_2 N66 N73 Gnd PadVdd outpad-notermLowPower
Xoutpad-notermLowPower_3 N68 N71 Gnd PadVdd outpad-notermLowPower

Xvideopad_1 N69 N62 FoldBias Gnd PadVdd widepad
Xvideopad_2 N67 N60 FoldBias Gnd PadVdd widepad
Xvideopad_3 N65 N60 FoldBias Gnd PadVdd widepad
Xvideopad_4 N63 N48 FoldBias Gnd PadVdd widepad
Xvideopad_5 N61 N46 FoldBias Gnd PadVdd widepad
Xvideopad_6 N57 N59 FoldBias Gnd PadVdd widepad
Xvideopad_7 N53 N55 FoldBias Gnd PadVdd widepad
Xvideopad_8 N49 N51 FoldBias Gnd PadVdd widepad
Xvideopad_9 N47 N47 FoldBias Gnd PadVdd widepad
Xvideopad_10 N45 N43 FoldBias Gnd PadVdd widepad
Xvideopad_11 N41 N43 FoldBias Gnd PadVdd widepad
Xvideopad_12 N39 N39 FoldBias Gnd PadVdd widepad
Xvideopad_13 N33 N36 FoldBias Gnd PadVdd widepad
Xvideopad_14 N30 N31 FoldBias Gnd PadVdd widepad
Xvideopad_15 N26 N27 FoldBias Gnd PadVdd widepad
Xvideopad_16 N23 N22 FoldBias Gnd PadVdd widepad
Xvideopad_17 N17 N19 FoldBias Gnd PadVdd widepad
Xvideopad_18 N15 N15 FoldBias Gnd PadVdd widepad
Xvideopad_19 N9 N11 FoldBias Gnd PadVdd widepad
Xvideopad_20 N5 N7 FoldBias Gnd PadVdd widepad
Xvideopad_21 N1 N3 FoldBias Gnd PadVdd widepad

* End of main circuit: chipPlus
Appendix C

CD

The CD contains the *.tex files, dvi/ps/pdf version of the thesis, the schematics in Sedit, the layout in Ledit, Tspice netlists and test benches, simulation results, the lens tool, some related papers and pictures.