Abstract

The learning and classification of natural stimuli are accomplished by the animal brain with remarkable ease, even when the input is noisy or incomplete. Stand-alone, low-power artificial systems designed for robust reproduction of these capabilities could be efficiently utilized for a wide range of applications. Specifically, real time classification of complex patterns could lead to major advancement in the fields of prosthetics, autonomous robotics and brain-machine interfaces.

Various artificial neural network models have already been developed for applications related to pattern classification. These models are typically simulated in high speed digital computers that function in a fundamentally different way compared to biological neural networks. In contrast to the parallel analog computation and asynchronous event based communication in the brain, digital Very Large Scale Integrated (VLSI) silicon processors are synchronous, serial in operation, and far less power efficient. Computational elements in biology (e.g. neurons and synapses), unlike the ones in general purpose processors, are imprecise and unmatched, yet biological systems interacting with the natural environment exhibit a high degree of robustness, fault tolerance, and self adaptability. Nevertheless, it is recognized that the basic elements of the neural substrate and that of silicon technology obey similar physical principles. This similarity has led to an alternative approach, to the standard digital one, of building large networks of silicon neurons and synapses in VLSI using hybrid analog-digital circuits. Following this approach massively parallel and fault tolerant hardware devices can be built, which are well suited for emulating the properties of the spike-based synaptic plasticity, the root of learning and classification, observed in biology. Such artificial neural systems, whose architecture and design principles are based on those of biological nervous systems, are called *neuromorphic systems*.

In this project a hybrid analog-digital neuromorphic hardware device was built that exhibits memory formation and classification in real-time and with minimal power consumption. The system achieved a robust event-based inter-chip communication using formal asynchronous circuit design techniques. The dynamics of the silicon synapse, responsible for the analog processing, are based on a novel spike-based supervised learning mechanism recently proposed in the literature. Unlike classical neural network models, whose performance depends critically on the unrealistic feature of unbounded synaptic weights, this model incorporates synapses with limited analog resolution and bistable long term modification, both suitable for a VLSI implementation. During learning, the synaptic weights are modified only when necessary, i.e. as long as the current generated by all the stimulated plastic synapses does not match the output desired by the supervisor, allowing the device to classify highly correlated patterns.

Real-time classification performance of complex patterns of mean firing rates was quantitatively assessed using this VLSI device. The circuits responsible for synaptic plasticity and their dependence on pre- and post-synaptic signals were extensively characterized. The results include experimental data describing the behavior of the chip in classifying random uncorrelated binary patterns and determining the memory capacity of the network. This work demonstrates for the first time robust classification

of highly correlated spike patterns on a silicon device, and shows how the scaling properties of the system match those of the theoretical model it is based on.

The VLSI system exhibited superior performance, in terms of storage capacity and complexity of the patterns stored, when compared to state-of-the-art spike based learning chips. It could successfully learn graded and corrupted patterns paving the way for classification of realistic spike trains from neuromorphic sensors or from nerve cells. The results obtained in this project show how devices of this kind can become ideal candidate for low-power biomedical applications or for integration into multi-chip spike-based neuromorphic systems.