

Analog VLSI Model of Locust DCMD Neuron Response for Computation of Object Approach

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In this paper, we present an analog VLSI (aVLSI) architecture that implements a functional model of the locust descending contralateral movement detector (DCMD) neuron, based on recently published results. We describe its architecture and analog circuits that implement its critical computational modules. We also provide an analytical closed-form solution for some of the circuits proposed and verify the validity of our analysis both through circuit simulations and experimental data obtained from an aVLSI test chip. This work shows that the circuits here proposed can be used to build hardware devices to model DCMD response curves. Having complete control over the hardware system, neurophysiologists would then be able to measure in real time properties of looming stimuli and outcome of the neuromorphic model, while simultaneously performing the experiment on the real biological system.

1 Introduction

Behavioral and physiological evidence supports the hypothesis that insects detect impending collisions with surfaces or predators by using motion cues present in their visual field. It is believed that the locust neural circuitry responsible for the reaction to looming stimuli¹ differs from the one that measures time to contact which may be present in other insects and birds^{2,3}. While computation of time-to-contact may be crucial for landing or diving tasks, the algorithm implemented by the locust neural circuitry appears to be optimized for avoiding obstacles and preventing collisions while the locust is flying in a dense swarm¹. Recently, the neural circuitry that processes visual data and drives the DCMD neuron of the locust, has been an active topic of discussion^{4,5}. The DCMD is a wide-field motion sensitive visual neuron, present in the brain of the locust, that connects to motor units thus triggering escape or avoidance responses⁶. This neuron generally responds to different types of novel motion stimuli, but generates a robust sustained activity preferentially for approaching objects⁷. In⁴, the authors propose a novel interpretation of experimental data, which differs from (but doesn't contradict) interpretations previously proposed⁸. It has been argued that data and interpretations might differ because of different experimental setups or because of different parameter settings used for generating looming stimuli⁵.

In this paper, we present a set of aVLSI circuits which may be used as

functional building blocks to implement neuromorphic models of collision detectors. These systems could be used as helpful modeling tools for testing in real-time different hypotheses, while simultaneously measuring in a controlled way the characteristics of looming stimuli and keeping track of internal model parameters. Depending on the validity of the model implemented, the internal parameters might even represent physical signals not accessible in the real biological system (for example, activities of different populations of neurons present in the visual areas that project to the LGMD and DCMD).

The set of circuits described here was used to implement the algorithm proposed in ⁴. Nonetheless, the same circuits could be used as basic building blocks (*e.g.* adaptive photoreceptors, multiplier circuits, *etc.*) for implementing different models of the locust DCMD response.

2 DCMD response data fitting

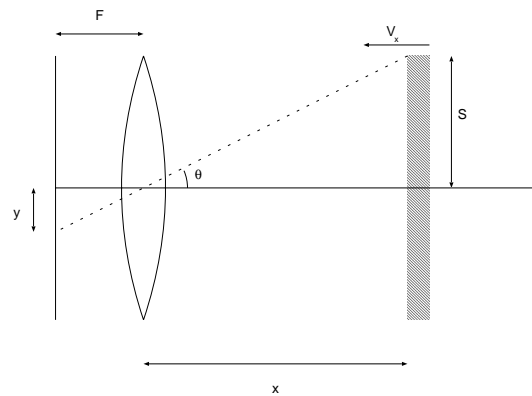


Figure 1: Example of experimental setup for measuring responses to looming stimuli.

Fig. 1 represents a scheme of an experimental setup for measuring DCMD responses to looming stimuli. The size of the object, S , and its velocity in the x direction, V_x , are kept constant. F is also a constant parameter representing the focal length of the lens. θ is the angle subtended by image size measured at the focal plane. Typically though, mechanical systems that move objects towards the focal plane are not used much. Approaching objects are simulated by displaying expanding squares or circles on monitor or oscilloscope screens at a distance F of the locust's eye.

The responses of DCMD to approaching objects, as measured in ⁴, were well fitted by the equation:

$$f(t) = C|\dot{\theta}(t - \delta)|e^{-\alpha\theta(t-\delta)}, \quad (1)$$

where $\theta(t)$ represents the stimulus size and $\dot{\theta}(t)$ its angular velocity. C is a proportionality constant scaling the function to measured firing rates, whereas α and δ characterize the location of the peak DCMD response and its lag with respect to the stimulus respectively (see Fig. 2).

From trigonometric relationships and derivative rules, it can be shown that:

$$\theta(t) = \arctan\left(\frac{S}{V_x} \cdot \frac{1}{t}\right) \quad \text{and} \quad \dot{\theta}(t) = \frac{-SV_x}{S^2 + V_x^2 t^2} \quad (2)$$

The function $f(t)$ of equation 1 can then be plotted taking into account different experimental conditions (*i.e.*, different values of F , V_x and/or S). Initially, when stimulus size is relatively small, the velocity component ($\dot{\theta}$) is the dominant term and $f(t)$ increases. As the size component (θ) gets bigger, the exponential term becomes dominant and $f(t)$ peaks and begins to decrease rapidly (see Fig. 2).

3 Measuring Expanding Motion

An essential part of the computation carried out by proposed models of object avoidance in the locust ^{4 8 1} is the part dealing with the measurement of expanding motion. To detect approaching objects and eventually compute time-to-contact, it is necessary to measure the expansion rate of the stimulus image on the retina.

In ⁹, the authors propose a simple algorithm for extracting from local velocity measurements integrative properties of the optical-flow field, such as rotation and expansion. The proposed algorithm, biologically inspired and (consequently) well suited to neuromorphic aVLSI implementation, is based on the 2D version of Gauss' divergence theorem: it sums over a closed contour the normal component of the optical flow, measured along the contour itself. A chip implementing this algorithm has already been designed in our labs ¹⁰. Such device uses twelve elementary velocity sensors, implemented by compact analog circuits ¹¹, arranged along a circle. Each velocity sensor measures the radial component of the stimulus velocity and sums its output current into one global common node. To measure expanding motion and the size of the stimulus projection on the retina, using the same principle, we would need to design an architecture like the one shown in Fig. 3. This would require a large

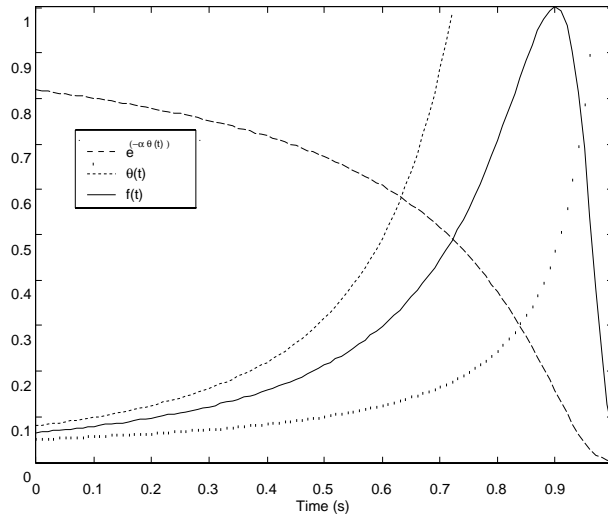


Figure 2: Plot of the function used to fit experimental data obtained from extracellular recordings of the DCMD neuron activity in response to looming stimuli. Parameter α was set to 4, while $\frac{S}{V_x}$ was set to 0.05. In this simulation, the impact time was set to $t = 1$ s. The functions have thus been plotted using $(1 - t)$ as independent variable.

area of the silicon die or an advanced fabrication technology. Being interested at the moment in testing the general validity of our ideas and in characterizing the individual circuits here proposed, we chose to limit the number of circuits on the chip and to implement only a radial subset of the architecture, as evidenced in dark gray on the right part of Fig. 3. This allowed us to use a low cost $2\mu\text{m}$ technology and a small chip size (of approximately $2\text{mm} \times 2\text{mm}$).

4 Hardware Implementation

We implemented a 1-D architecture containing 25 pixels, using a standard $2\mu\text{m}$ CMOS technology. Such an analog VLSI device measures size and velocity of moving stimuli and combines the results of these measurements to compute both the function $f(t)$ of equation 1 described in section 2, and its natural logarithm. The block-diagram of the analog VLSI system is shown in Fig. 4. On-chip adaptive photoreceptors respond to local contrast variations and provide parallel inputs to elementary velocity sensors and to size-computation circuits. The photoreceptors used are circuits based on a model of the invertebrate retina that can adapt to over six orders of magnitude in light amplitude

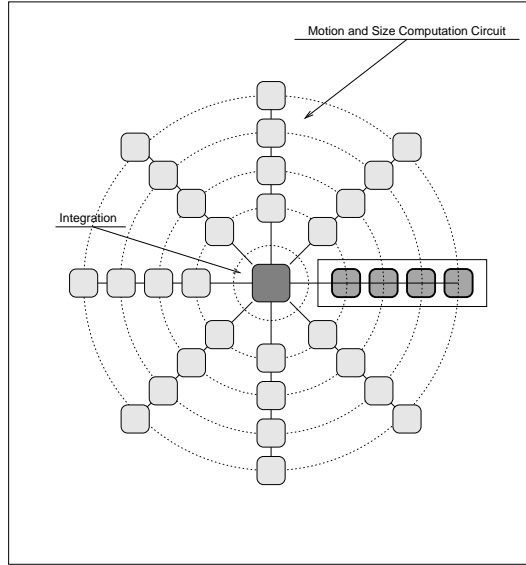


Figure 3: Architecture of a hypothetical system for measuring stimulus size and expanding motion exploiting the 2D version of Gauss' divergence theorem.

¹². The output of each photoreceptor is then thresholded and converted into a current (I_θ). This current increases proportionally with the number of photoreceptors progressively covered by the stimulus projection on the chip area. The velocity of the stimulus is computed locally (*i.e.*, at each pixel location) by elementary velocity sensors. These sensors are compact circuits, based on the Reichardt correlation algorithm that are able to respond to a wide range of stimulus velocities¹¹. To avoid ambiguities, we consider out of all the velocity measuring circuits, only the one whose output encodes the maximum velocity. This operation, carried out by a winner-take-all network¹³, exploits the fact that the stimuli used to test the model have increasing velocity with increasing size. The velocity signal is thus encoded by a single current value $I_{\dot{\theta}}$ directly proportional to the speed of the stimulus. The global motion signal ($I_{\dot{\theta}}$) and the signal encoding the size of the stimulus image on the chip area (I_θ) are fed in as input to two separate circuits. These circuits independently compute the product of $I_{\dot{\theta}}$ with an exponential function of I_θ (to implement $f(t)$ of equation 1) and the sum of the natural logarithm of $I_{\dot{\theta}}$ with I_θ (to implement $\log(f(t))$). One of the purposes of this work was in fact to evaluate which of these two circuits is best suited to the type of computation we are trying to

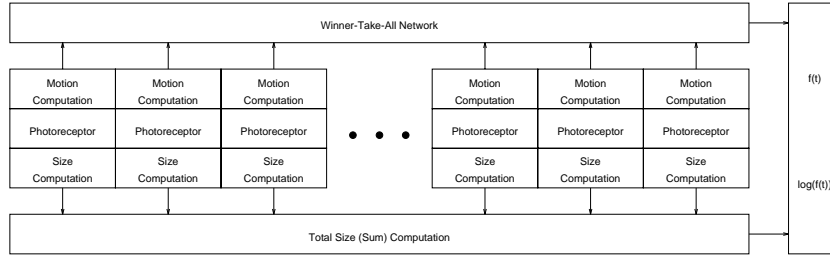


Figure 4: Block diagram of the analog VLSI system used to measure size and expansion rate of approaching objects. The photoreceptors transduce the luminous signal into voltage signal which are processed simultaneously by motion computation circuits and size computation circuits.

carry out.

4.1 Exponentials and products of currents

The circuit that computes the exponential of an input current and multiplies it with a second input current is shown in Fig. 5. It is a *current mode* circuit

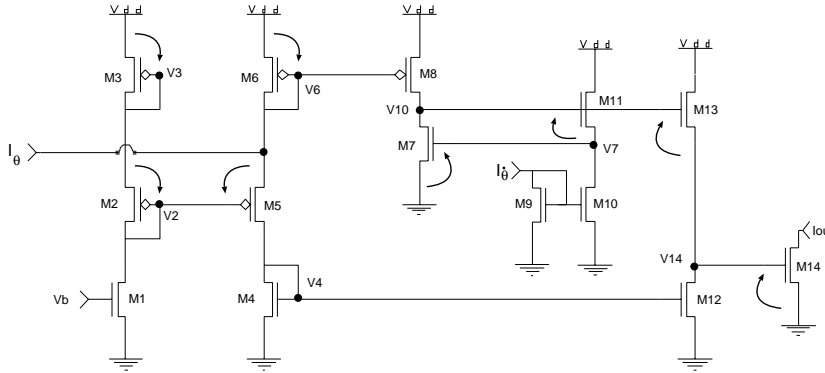


Figure 5: Circuit that computes the product of the exponential of an input current with a second (positive) current.

(*i.e.*, signals are represented as currents and voltages play only a minor role) that operates in the *subthreshold* domain¹⁴. In this domain MOS transistor gate voltages are typically lower than threshold voltages and the equation that characterizes MOS devices in saturation is:

$$I_d = I_0 e^{\kappa \frac{V_G}{U_T} - \frac{V_S}{U_T}}, \quad (3)$$

where I_d represents the transistor's drain current, V_G its gate voltage, V_S its source current and U_T the thermal voltage, equivalent to $\frac{kT}{q}$. The term κ is a coefficient that takes into account the *body* effect (appendix B of ¹⁵), non-negligible in this domain.

Thanks to the exponential relationship between gate voltage and drain current, we can analyze the circuit applying the *translinear principle*, an elegant and computationally powerful rule for current mode circuits. The principle states that in a closed loop containing an equal number of oppositely connected translinear elements, the product of the current densities in the elements connected in one direction is equal to the corresponding product for elements connected in the opposite direction.

If we assume that all transistors of Fig. 5 have the same geometries and we consider the loop containing transistors M3-M2-M5-M6, we obtain: $I_3 \cdot I_2 = I_5 \cdot I_6$, where I_n represents the subthreshold current flowing through the channel of transistor n . The current flowing through M3 equals the current flowing through M2, and both of them are equal to I_b , a bias current set by an external voltage V_b applied to M1. Moreover, the current flowing through M4 matches the current flowing through M5, which in turn can be expressed as $I_5 = I_6 + I_\theta$ (where I_θ is the input current representing the size of the stimulus projection on the chip). The loop equation can then be rewritten as: $I_b^2 = I_6 \cdot (I_6 + I_\theta)$. If we solve this equation for I_6 we obtain:

$$I_6 = \frac{\sqrt{I_\theta^2 + 4I_b^2} - I_\theta}{2} \quad \text{and} \quad I_5 = \frac{\sqrt{I_\theta^2 + 4I_b^2} + I_\theta}{2} \quad (4)$$

If transistor M8 is in saturation and matches well M6, I_7 will faithfully copy I_6 . Applying the inverse of equation 3 to transistors M4 and M7 we will then have:

$$V_7 = \frac{U_T}{\kappa} \log \left(\frac{I_6}{I_0} \right) \quad \text{and} \quad V_4 = \frac{U_T}{\kappa} \log \left(\frac{I_5}{I_0} \right) . \quad (5)$$

The differential voltage $V_7 - V_4$ will thus be a function linearly proportional to I_θ , with a variable slope α controlled by I_b (see Fig. 6):

$$V_7 - V_4 = \frac{U_T}{\kappa} \log \left(\frac{\sqrt{I_\theta^2 + 4I_b^2} - I_\theta}{\sqrt{I_\theta^2 + 4I_b^2} + I_\theta} \right) \approx -\alpha I_\theta . \quad (6)$$

The linear relationship will hold for all values of I_θ that satisfy $|I_\theta| < I_b$.

Let us now consider the loop containing transistors M7-M11-M13-M14. Application of the translinear principle to this loop will give $I_7 \cdot I_{11} = I_{13} \cdot I_{14}$. If we substitute I_{11} with I_θ , I_{13} with I_4 and I_{14} with I_{out} we obtain:

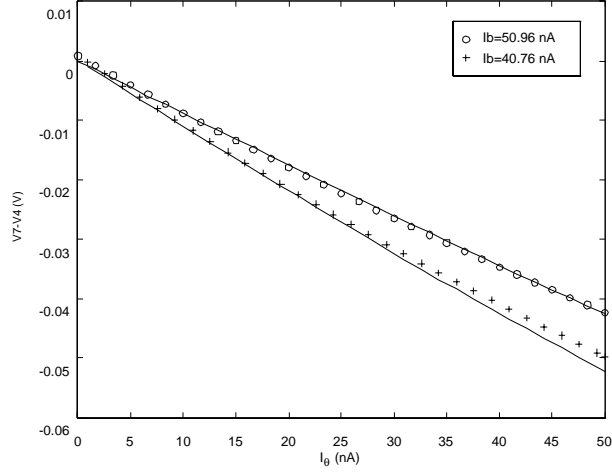


Figure 6: Simulation results of the circuit shown in Fig. 5, fitted with equation 6. Parameters κ and U_T were set to 0.6 to 27mV respectively.

$$I_{out} = I_{\dot{\theta}} \cdot \frac{I_7}{I_4} . \quad (7)$$

Applying the device equation (eq. 3) to I_4 and to I_7 we get:

$$I_{out} = I_{\dot{\theta}} e^{\frac{\kappa}{U_T}(V_7-V_4)} = I_{\dot{\theta}} e^{-\alpha I_{\theta}} . \quad (8)$$

This circuit thus directly implements $f(t)$ of equation 1, given input currents that represent stimulus size and stimulus velocity. It has the advantage of being a very elegant and compact circuit, but in order to function properly the transistors considered in the analysis must operate in saturation and remain in the subthreshold domain. Moreover the current mirrors must have good matching properties. These constraints place limits on the dynamic range of the input signals, which in some cases might be too restricting. An alternative approach is to consider the natural logarithm of $f(t)$.

4.2 Logarithms and sums of currents

Figure 7 shows the circuit used to compute the equation

$$\log(f(t)) = C' (\log(\dot{\theta}(t)) - \alpha \theta(t)) . \quad (9)$$

The current encoding the velocity of the stimulus, coming from the winner-take-all circuit, is converted into a voltage ($V_{\dot{\theta}}$). If the transistors operate in the right (subthreshold) domain, $V_{\dot{\theta}}$ will be a logarithmic function of the current (see equation 3). $V_{\dot{\theta}}$ is then fed in as input to a wide-range transconductance amplifier. The transfer function of this amplifier in the subthreshold domain is the following¹⁵:

$$I_{amp} = I_b \tanh \frac{\kappa(V_{THR} - V_{\dot{\theta}})}{2U_T}, \quad (10)$$

where I_b is a bias current set by the external voltage V_b and V_{THR} is a threshold voltage, also set externally. If we set V_b and V_{THR} appropriately, we can operate the amplifier in its linear range. Its output current will then be directly proportional to the input voltage $V_{\dot{\theta}}$ (encoding $\log(I_{\dot{\theta}})$). The n-type current mirror connected to the transconductance amplifier implements a half-wave rectification function, so that only positive currents are copied to the output. Subtraction of the positive current encoding $\log(I_{\dot{\theta}})$ with I_{θ} is performed at the output node, exploiting Kirchoff's current law.

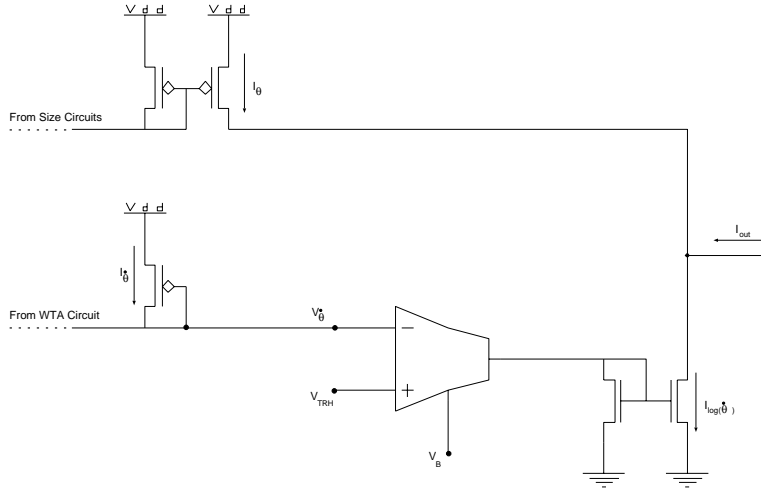


Figure 7: Circuit used to compute the sum of the current encoding the size of the stimulus projected on the chip's retina with the current encoding the logarithm of its velocity.

5 Experimental Results

To test the device here described, we had to generate appropriate motion stimuli that would give the illusion of looming or approaching objects. Having

to evaluate its functionality at a qualitative level and being concerned with aliasing problems and artifacts that might occur using monitors and computer generated stimuli (one probable source of the experimental controversy⁴⁵), we chose to use a mechanical apparatus as stimulus generator. The testing setup is composed of a rotating drum (with a white surface and a high-contrast edge drawn on it) and of a board containing the chip, the optics and additional electronics (*e.g.* for converting currents into voltages). Since we implemented only a 1-D subset of the complete 2-D retina chip of Fig. 3, we had to project edges with a profile given by the function $1/t$ to generate the appropriate illusion (see eq. 2).

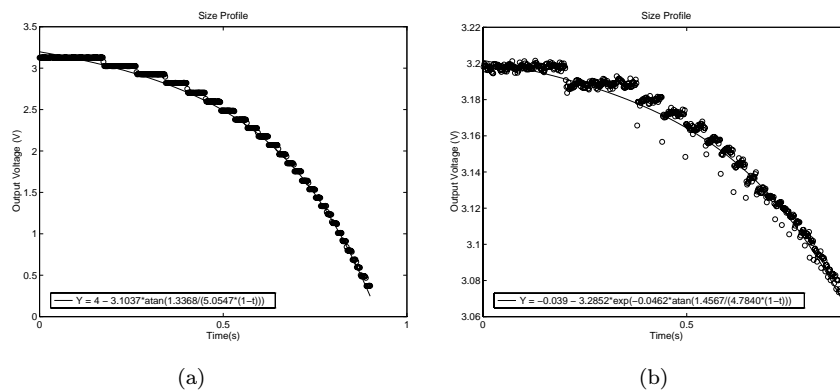


Figure 8: (a) Output of size-computing circuits fitted with a function that matches the expected profile of the size of a stimulus approaching the retina at a constant velocity; (b) Output of the circuit of Fig. 5 having set $I_{\hat{\theta}}$ to a constant value. The curve is well fitted by an exponential of the fitting function used in (a).

Figure 8(a) shows the output of the circuit of Fig. 7 with the transconductance amplifier switched off. The output current thus encodes simply the size of a stimulus, as it approaches the retina at a constant velocity. The chip data fits well the function $\theta(t)$ of eq. 2. Figure 8(b) on the other hand shows the output of the size-computing circuits processed by the circuit of Fig. 5 (with $I_{\hat{\theta}}$ externally fixed to a constant value). This output current (converted into voltage by an external sense amplifier) should be proportional to an exponential function of the size profile. This is confirmed by the fitting function plotted in Fig. 8(b) and also by Fig. 9, which shows on the same plot the output of both circuits (again, ignoring motion signals).

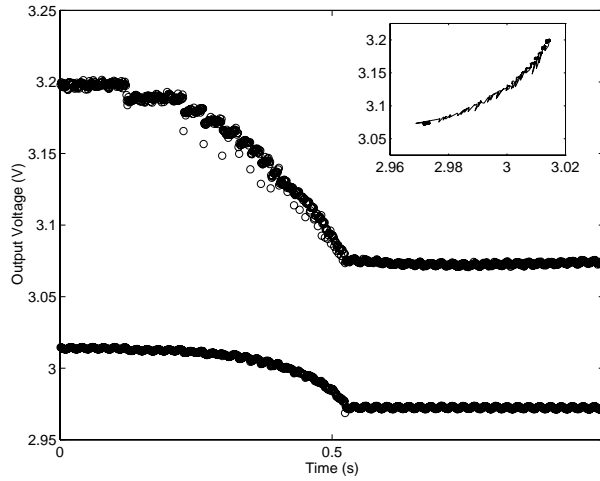


Figure 9: Output of size computing circuits (bottom plot) and of exponential-of-size computing circuit (top plot). The inset, containing a plot of the top curve versus the bottom curve, shows their exponential dependence.

Experimental data confirmed the correct behavior of both circuits processing signals encoding the size of the stimulus. However, it also showed how the circuit implementing the multiplication of exponentials of Fig. 5 is more noisy and produces small oscillations in its output (see Fig. 8(b)). This oscillatory behavior is present also when we apply a motion signal to the system. For this reason, in the following paragraphs we will take into account only the circuit of Fig. 7.

Due to a technical mistake in the layout of the elementary velocity sensors, the motion computation circuits did not work correctly. However we know from our experience with previous chips, developed in our own labs^{11,10}, that such velocity sensors yield good performance figures. Being unable to provide the correct velocity signal, we had to use a function generator and connect it to an additional input of the winner-take-all circuit (receiving inputs also from the array of non-operative velocity sensors). In such a way, we were able to simulate only a linear velocity profile, instead of the desired one, expressed in eq. 2. Figure 10 shows the output of the circuit of Fig. 7 with the transconductance amplifier working in its linear range, in response to the size signal computed from the chip and the velocity signal provided by the function generator. Even if the externally generated velocity signal is not realistic (*i.e.*, it doesn't correspond to the correct $\dot{\theta}(t)$ for the given $\theta(t)$), the measured data fits well the

theoretical function that the circuit is designed to implement (corresponding to eq. 9). As with the model proposed in ⁴, as long as $\theta(t)$ is small, the term containing $\dot{\theta}(t)$ is dominant. As soon as the size of the stimulus starts getting big enough, the term containing $\theta(t)$ becomes dominant and the the output signal starts to decrease rapidly.

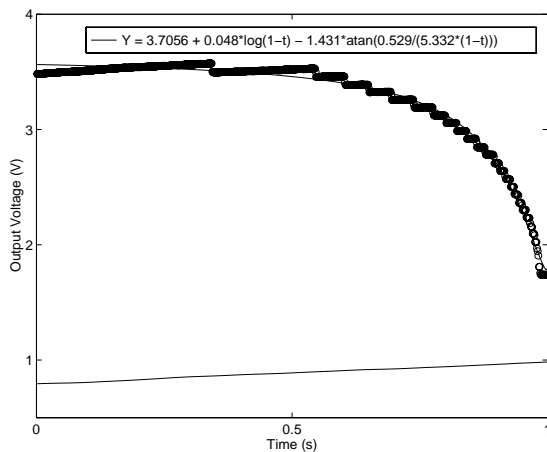


Figure 10: Output of the circuit of Fig. 7 with both size and velocity signals active. The bottom plot represents the velocity signal, artificially generated, using a function generator. The solid line in the top plot represents a fit function which matches the profile expected from eq. 9.

6 Conclusions

In this paper we described a VLSI device containing test circuits that implement a functional model of the locust obstacle avoidance mechanism. We evaluated the performance of these circuits for a simple 1-D architecture. Approaching objects were simulated using a mechanical system and an optical illusion. This demonstrated the correct behavior of the critical circuits implementing multiplicative, exponential and logarithmic operators. Using these circuits, we intend to design a full 2-D architecture, which will implement a more complex and realistic model of the locust DCMD neuron. Such a device will initially be used as a tool to test the validity of different models for the computation of object approach by DCMD; for comparing its output in real-time with neurophysiological data; for measuring the properties of computer gen-

erated looming stimuli (as we have control over parameters such as frequency sensitivity of its photoreceptors). On a longer time scale, we intend to further develop these devices to investigate possible uses in the automotive industry. The same mechanism responsible for triggering escape responses in the locust neural circuitry could be indeed exploited for developing compact, low power aVLSI devices to be used as *intelligent sensors* for obstacle avoidance tasks or for providing additional information to automotive air-bag systems, to improve their overall performance and decrease their false-alarm rates (compare swarms of locusts flying in the desert to cars driving in freeways).

Acknowledgments

Many of the circuits used in the system here described were originally developed at Caltech in Professor's Mead and in Professor's Koch labs. I would like to acknowledge Fabrizio Gabbiani and Claire Rind for exchanging their views and ideas on models of DCMD collision avoidance. This work was supported by Swiss National Science Foundation. Fabrication of the integrated circuits was provided by MOSIS.

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