A Programmable Clock Generator HDL Softcore

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***Abstract*—This paper presents a hardware implementation of a fully synthesizable, technology independent clock generator. The design is based on an ADPLL architecture described in VHDL and characterized by a digital controlled oscillator with high frequency resolution and low jitter. Frequency control is done by using a robust regulation algorithm to allow a defined lock-in time of at most 8 reference cycles. ASICs in CMOS AMS 0,35um and UMC 0,13um have been manufactured and tested. Measurements show competitive results to state-of-the-art mixed signal implementations.**

I. INTRODUCTION

The fast creation of complex system on chip (SOC) designs consisting of several intellectual property (IP) cores is state of the art for standard digital functionality [1]. A problem in this context are mixed-signal subblocks within the chip. These are highly technology dependent and a time consuming re-design is necessary when technology or application area are modified [2].

An essential part of most modern digital circuits is a clock generator. This could be used to generate a high working frequency out of a much lower reference. It is also possible to regulate this output frequency dynamically with regards to low power design. The usage of a phase locked loop (PLL) architecture is a very effective way to form this function block. A PLL tries to synchronize a reference frequency with the output frequency of an oscillator by adjusting the latter.

Classical PLL implementations rely on analog components [1]. Because of this they are not suited for usage as an IP core. As mentioned above an extensive re-design has to be done any time the technology or the frequency specification is changed. A new approach are All-Digital PLLs (ADPLL). Their hardware implementation consists completely of digital standard cells [1,2]. The phase detector, loop filter and frequency divider can easily be described in a high level hardware description language (HDL) to form a technology independent softcore [1,2,3]. More difficult to implement is the digital controlled oscillator (DCO). The DCO designs presented in [1,4] still require a time-consuming manual fine tuning depending on the target library to meet the specified frequency and jitter specification. Compared to that, the clock generator design presented in this paper could be implemented in the same fast and easy way as a typical IP core in every standard digital synthesis-based design flow. This is realized by a combination of the standard-cell based low jitter DCO presented in [3,5] and a robust frequency regulation algorithm based on successive approximation, as described in the following.

II. ADPLL CONCEPT DESCRIPTION

The main application of such an ADPLL will be in supplying a clock reference for distributed digital processing systems on an SoC, based on one master reference clock. This design target necessitates a very high accuracy with respect to the master clock.

A. Architecture

The ADPLL is based on an architecture documented in a recent patent [5]. Long-term frequency stability and fine-tuning of the output signal is achieved via switching between two adjacent length using a fractional divider (here called modulo M unit). Analytical jitter descriptions of this architecture have been derived in reference [3].

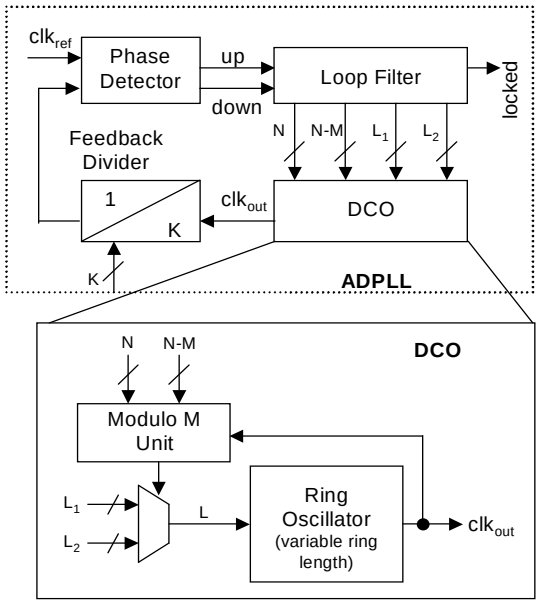

Figure 1. Architecture of the discussed ADPLL

This work was supported by the European Union as integrated project FACETS (Nr. FP6-015879) in the framework of the Information Society Technologies program.

Since the clock is intended for digital processing systems, no analog fine tuning of the DCO delay elements is required. Besides long term accuracy, the only additional requirement is that the jitter is small enough with respect to the clock period not to violate timing constraints of digital circuits supplied by this clock. This can be assured by using fast single elements in the DCO chain, where switching between two adjacent length does not substantially alter the basic clock period (see also Fig. 5).

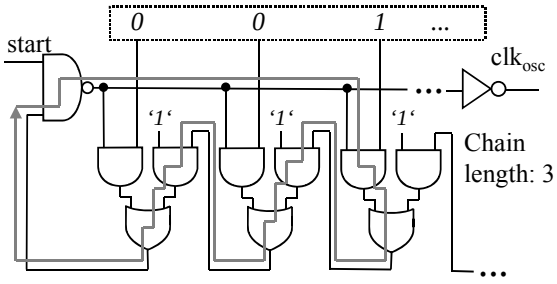

Figure 2. Oscillator chain for a one-hot coded length of three

As shown in Fig. 2, the DCO chain consists of AND-OR combinations which can be easily set to a defined chain length via a one-hot coded configuration word and have low propagation delay [6,3]. The basic building blocks as detailed above are the same for both presented implementations of the PLL. Compared to the 0.35 µm PLL, the 0.13 µm PLL has been designed for a higher clock reference, so the multiplication factor of the feedback divider is not as large. Additionally, the 0.13 µm PLL features a programmable divider between PLL output and the clock output pin of the IC, since its output frequency range is too high to send directly of chip.

B. Functional Description

In extension of the patented features [5], the architecture presented here is characterized by a technology independent, successive approximation type DCO frequency acquisition, with coarse tuning of the ring length and subsequent fine tuning of the fractional divider ratio:

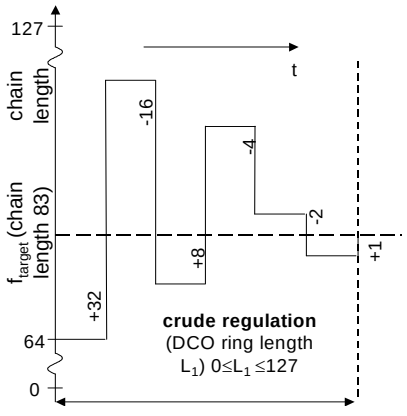

Figure 3. Frequency acquisition and control scheme of the ring length tuning.

Usually, the target frequency will correspond to an intermediate chain length between two discrete length L_1 and L_2. Once this chain interval has been found according to the procedure in Fig. 3, a similar successive approximation is used to find the ratio N/M of the modulo M unit:

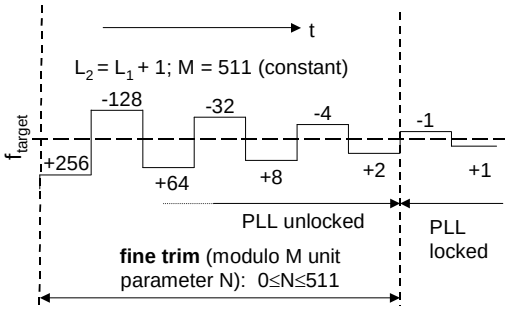

Figure 4. Frequency acquisition and control scheme of DCO

If the regulation is down to switching the last bit of N, the PLL has achieved a lock on the frequency. The DCO is adjusted with both rising and falling edges of the reference clock, resulting in a lock acquisition of less than 8 reference cycles. Once the fine trim is achieved, the modulo M unit simply counts the output clock cycles at both of the length L1 and L2 which are closest to the target frequency, switching between the two at the appropriate ratio to ensure the overall accuracy of the output frequency. Fig. 5 shows this switching principle through a histogram of the clock periods in PLL mode for both designs (measurement data).

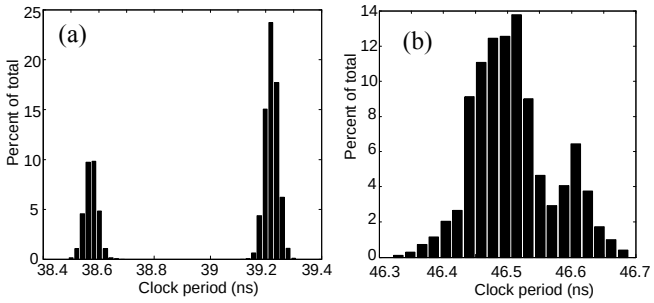

Figure 5. Histogram of sample clock periods for (a) 0.35 µm PLL and (b) 0.13 µm PLL.

As can be seen, the output frequency divider of the 0.13 µm PLL tends to slightly mask the single periods of the DCO chain, drawing the two period distributions together.

The modulo M unit is central to the idea of long term accuracy of the PLL output with respect to the reference clock. Since it governs the fine tuning of the output clock frequency and its working is entirely digital and thus free of error, relative clock accuracy can be extended arbitrarily by increasing the counter length of the modulo M unit. The only penalty for this extension is the increased lock time of the fine trim as shown in Fig. 4.

As denoted by the continued switching of the last bit of N in Fig. 4, the frequency regulation is continually active, ensuring a fast lock reacquisition if the lock on a target

frequency is lost (i.e. through temperature variations which affect DCO delay times). This is detected by an overflow of the modulo M unit, which then refers regulation back to the successive approximation.

III. MEASUREMENT DATA

A. Power consumption

The effect of switching between two adjacent ring length for intermediate frequencies can be observed from the 'jittery' curve in Fig. 6. If the target frequency is directly between two ring delays, the switching frequency of the fractional divider is highest, resulting in the local maxima of the power draw, when compared to the fixed chain-length oscillator mode.

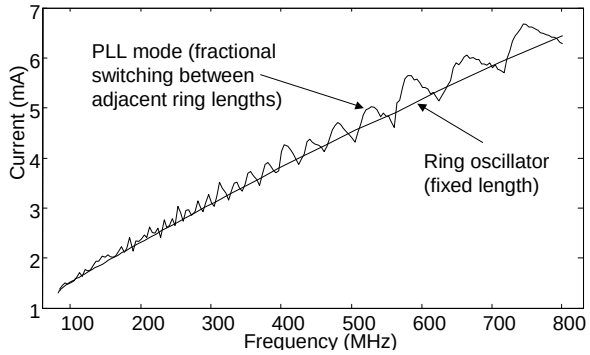

Figure 6. Current consumption as function of frequency for 0.13 µm PLL

Compared to the patented version, the fine tuning is done at the reference frequency, which drastically reduces the power dissipation. As can be seen from Fig. 6, the power requirements of the fractional divider are small compared to the linear scaling of DCO ring current with ring frequency. The total power draw of the circuits can be estimated as follows:

$$P_{tot,35} = 1.32mW + 145\frac{\mu W}{MHz}$$
$$P_{tot,13} = 1.9mW + 11\frac{\mu W}{MHz} \quad (1)$$

The scaling effect of digital power draw for shrinking technology sizes is evident from the above equations. The 0.13µm PLL has less than one tenth the frequency-dependent power requirements of the 0.35µm PLL.

B. Spectral Performance

PLL performance is often judged with respect to the spectral components within the clock jitter, especially if this PLL is meant for Radio Frequency (RF) applications [7]. Since our PLL has been optimized along different targets (i.e. high accuracy digital systems clock), its spectral performance is not sufficient for RF designs. However, we include the relevant dBc/Hz measurement for reasons of completeness and because it is of interest how effects of the modulo M unit show up in the jitter output spectrum:

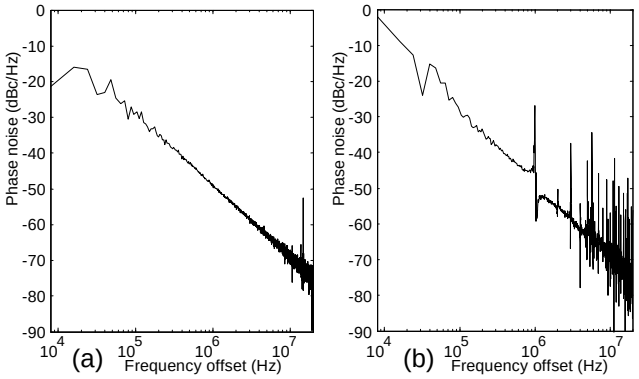

Figure 7. Phase noise (dBc/Hz) of DCO chain at fixed length corresponding to 91MHz (a) and PLL mode at 85 MHz with a reference clock frequency of 10 MHz

The phase noise of the ADPLL is very high compared to mixed-signal designs [7]. One reason is the usage of fast standard cell digital gates in the DCO chain, which have a high jitter compared to their mean delay times even for a fixed chain length, see Fig. 7 (a). When the DCO is used in PLL mode, additional jitter is introduced through the switching, especially around the reference frequency. This is due to the modulo M unit operating at the reference clock.

C. Aspects of Automated Digital PLL Design

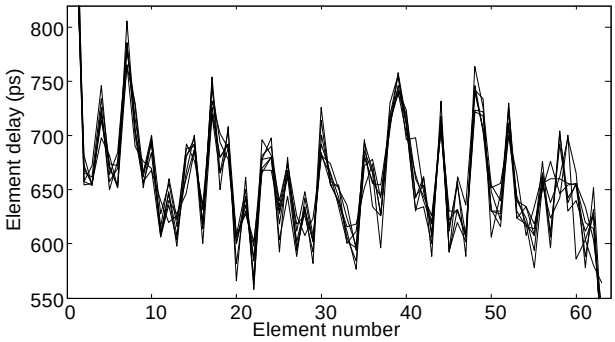

Figure 8. Delay of DCO elements in chain, measurement curves for several 0.35 µm ICs overlaid.

The matching between different sample ICs of the 0.35µm PLL implementation in Fig. 8 shows that a large proportion of the jitter is due to the haphazard placement of the DCO elements rather than process variations. By using additional constraints to regularize placement and balance wire length within the place-and-route routine, the jitter due to delay variations between consecutive DCO delay gates can be substantially reduced. If the layout-caused jitter from Fig. 8 is subtracted from the measured data, the peak-peak jitter can be reduced to the values in parenthesis in table 1.

D. Comparison with Recent Designs

Further measurement data is summarized in table 1. As can be seen, most parameters are comparable or superior to recent examples. In addition the described architecture is

TABLE I. PERFORMANCE COMPARISON: MEASUREMENTS OF DESCRIBED PLL'S AND RECENT LITERATURE

Parameter	Proposed ADPLL		[1]	[4]
Process	0.35 µm CMOS	0.13 µm CMOS	0.18 µm CMOS	0.18µm CMOS
Area	0.204mm^2	0.027mm^2	0.019 mm^2	0.16mm^2
Approach	Cell-Based synthesizable	Cell-Based synthesizable	Cell-Based, mixed analog/digital DCO	Cell Based, mixed analog/digital DCO
Power Dissipation	41mW@274MHz	7.4mW@500MHz	100mW@500MHz	15mW@378MHz
Max. Lock Time	<8 cycles	<8 cycles	< 272 cycles	<75 cycles
Output Range	22.1 ~ 274 MHz	84 ~ 800 MHz	140 ~ 1030 MHz	2.4 ~ 378MHz
Supply Voltage	3.3V	1.5V	3.3 V	1.8V
Peak-Peak Jitter	1000ps (730ps)	870ps (690ps)	143 ps	208ps@134.7MHz
Mult. Factor	1 ~ 65536	1 ~ 255	/	4 ~ 13888

fully synthesizable. For example, resynthesizing the 0.35µm architecture in 0.13µm and adjusting the multiplication factor for the new application took three man-days. The residual jitter is still high, but entirely sufficient for the target application.

IV. CONCLUSION

We present an ADPLL design optimized for portable data logging and processing systems. The design achieves a fast multiplication factor adjustment to enable dynamic low power modes, wide range of multiplication factors to compensate for off-the-shelf reference clocks, and low power consumption. Long term clock precision with respect to reference signal is assured, and the design is based entirely on digital standard cells for easy portability across different CMOS technologies. A chip microphotograph of the 0.35µm PLL on an SoC IC is shown in Fig. 9:

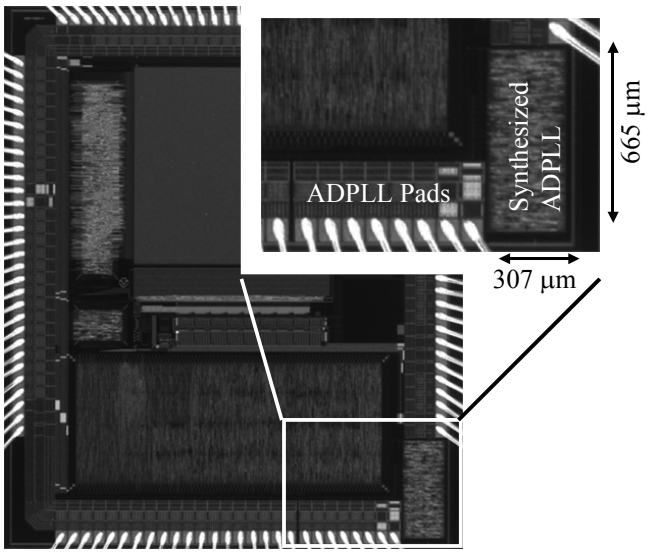

Figure 9. Chip microphotograph of the 0.35 µm PLL (lower right corner) realized as part of a preprocessing pixel sensor SOC (backdrop)

In [8], a method for fast PLL lock acquisition is presented which achieves lock times comparable with our successive approximation. However, the design in [8] relies on analog models of the DCO chain, which have to be coded into the frequency regulation algorithm, obstructing portability of this design across changing technologies. In contrast, the successive approximation used herein is in keeping with a technology-independent design, since it relies on ordinary clock cycle counter functionality to achieve its frequency lock.

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