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Implementing homeostatic plasticity in VLSI networks of spiking neurons

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Abstract— Homeostatic plasticity acts to stabilize firing activity in neural systems, ensuring a homogeneous computational substrate despite the inherent differences among neurons and their continuous change. These types of mechanisms are extremely relevant for any physical implementation of neural systems. They can be used in VLSI pulse-based neural networks to automatically adapt to chronic input changes, device mismatch, as well as slow systematic changes in the circuit’s functionality (e.g., due to temperature drifts). In this paper we propose analog circuits for implementing homeostatic plasticity mechanisms in VLSI spiking neural networks, compatible with local spike-based learning mechanisms. We show experimental results where a homeostatic control is implemented as a hybrid SoftWare/HardWare (SW/HW) solution, and present analog circuits for a complete on-chip stand-alone solution, validated by circuit simulations.

I. INTRODUCTION

Systems interacting with the real world in an intelligent way need to modify themselves to learn and adapt to the statistics of the input signals, while maintaining their activity within functional ranges, to keep a stable and homogeneous computational substrate. In biological neural systems these opposing requirements are driven by local learning mechanisms that induce changes in the weights of individual synapses of the network, acting on time scales ranging from milliseconds to minutes, and by global stabilizing homeostatic mechanisms that operate on longer time scales (ranging from minutes to hours) and are not synapse-specific [1], [2]. These mechanisms act to stabilize learning processes and ensure a homogeneous computational substrate despite the inherent differences between neurons, the continuous turnover of their constituents and chronic changes of their environment [2].

Despite many implementations of Hebbian learning mechanisms that comprise forms of stabilization [3] and synaptic competition [4], [5] have been proposed, very few attempts have been made to implement explicit global homeostatic plasticity mechanisms, in parallel with classical local learning ones [6]. However, it has been recently argued that the interplay between local Hebbian and global homeostatic processes can have complementary roles [5], or even important synergistic effects [6], allowing for complex behaviors, such as independent component analysis, which would not be possible with either mechanisms alone.

In parallel to the theoretical studies on plasticity in neural networks, a large research effort has been recently devoted to the construction of biologically inspired pulse-based neural systems, particularly via the VLSI neuromorphic approach [7]–[12]. However, the focus has been primarily on the implementation of local short-term spike-based learning algorithms [7], [8], [13], [14], with comparatively little work devoted to global long-term stabilizing processes [15]. In VLSI implementations of neural networks homeostasis could be used to implement a form of automatic gain control to compensate for inhomogeneities due to device mismatch, slow changes in the physical properties of the circuits arising due to temperature drift, or sudden changes in the overall levels of activity in the network (e.g., due to activation or inactivation of sub-modules).

Here we propose a set of neumorphic circuits and methods that implement in parallel both local spike-based plasticity mechanisms and global stabilizing homeostatic mechanisms. The specific form of homeostatic plasticity that we consider in this work is denoted as “activity dependent synaptic scaling” [1]. This multiplicative scaling mechanism acts globally, on the entire population of synapses, and does not affect the relative differences between the synaptic weights, typically induced by local learning mechanisms.

We first demonstrate a mixed SW/HW homeostatic control system that supports both “fast” spike-based learning rules, and “slower” homeostatic synaptic scaling mechanisms (Section II), and subsequently present a novel analog circuit, based on control theory lag compensation technique, that implements the homeostatic control algorithm developed and that can be integrated in future neural network chips, for stand-alone VLSI solutions (Section III). To our knowledge, this is the first physical system capable of implementing homeostatic plasticity in parallel with spike-timing dependent plasticity.

II. HOMEOSTATIC CONTROL IN SPIKING SILICON NEURONS

In most pulse-based neural network chips, neurons have an architecture of the type shown in Fig.1: a series of synapses receive separate spiking input signals and produce output currents that are integrated by the soma circuit. The soma is typically an integrate-and-fire (I&F) neuron that produces an output spike train at a rate proportional to the sum of
The current amplitude is set by \( \text{generate the output current} \). Fig. 2. Diff-Pair Integrator synapse. Input spikes activate the circuit and post-synaptic spikes are used to modulate global synaptic scaling parameters. Fig. 1. General homeostatic control scheme for a typical VLSI integrate and fire neuron: synaptic input spikes drive “fast” spike-based learning circuits; post-synaptic spikes are used to modulate global synaptic scaling parameters for stabilizing the neuron’s spiking activity. An external constant current can be injected in the soma to modulate its baseline activity.

Fig. 2. Diff-Pair Integrator synapse. Input spikes activate the circuit and generate the output current \( I_{\text{syn}} \) that has an exponential profile over time. The current amplitude is set by \( V_w \) and \( V_{\text{thr}} \), while its time constant is set by \( V_T \).

all its synaptic currents. While local spike-based plasticity circuits can be used to implement Hebbian-type learning in each synapse block, the homeostatic control block globally adapts the gain of all the synapses afferent to that neuron, to keep its average firing rate close to a target frequency.

A. The Diff-Pair Integrator

A circuit that can implement both global synaptic scaling and local spike-based learning, is the “Diff-Pair Integrator” (DPI) synapse [16], shown in Fig. 2. Input spikes activate the \( M_{\text{pre}} \) transistor and allow current to flow through the differential pair. The \( M_{\text{w}} \) transistor weighs the input current depending on the magnitude of the \( V_w \) voltage. This voltage can be modified by spike-driven synaptic plasticity circuits, such as the ones proposed in [7], [8], [13], [14], [17], to implement local learning rules. The voltage \( V_{\text{thr}} \) sets a second independent gain parameter, used for our homeostatic control algorithm, while the voltage \( V_c \) determines the duration of the Excitatory Post-Synaptic Current (EPSC) \( I_{\text{syn}} \).

Assuming all transistors operate in the subthreshold regime and are saturated, the DPI’s transfer function is [16]:

\[
\tau \frac{d}{dt} I_{\text{syn}} + I_{\text{syn}} = \frac{I_w}{I_g} I_{\text{syn}} - \frac{I_{\text{syn}}}{I_g} \frac{I_{\text{syn}}}{I_g}
\]

where \( \tau \) = \( U_T C_{\text{syn}}/\kappa I_s \), \( U_T \) is the thermal voltage, \( \kappa \) is the subthreshold slope factor, \( V_{dd} \) the power supply voltage, and \( I_g \) is a \textit{virtual} current not tied to any MOSFET in the circuit defined as \( I_g = I_0 e^{-\frac{\Delta V_{DD} - \Delta V_{\text{th}}}{V_T}} \).

For \( I_{\text{syn}} \gg I_g \), the non-linear eq.(1) reduces to a classical low-pass filter equation:

\[
\frac{\tau}{dt} I_{\text{syn}} + I_{\text{syn}} = \frac{I_w}{I_g} I_{\text{syn}} \tag{2}
\]

Under these assumptions, when the synapse receives input spike trains of mean frequency \( f_{in} \), its steady-state mean output current can be described as:

\[
\langle I_{\text{syn}} \rangle = \frac{I_g I_w}{I_g} \frac{f_{in}}{I_g} \tag{3}
\]

B. Homeostatic control in a mixed SW/HW system

In a first stage, to explore different control strategies, we implemented homeostasis as a software algorithm on a workstation interfaced to a VLSI chip comprising a low-power I&F neuron [7] and a DPI synapse [16]. The chip was fabricated using a standard 0.5µm CMOS technology via the MOSIS consortium. The workstation was used to send sequences of spikes to the DPI synapse, and to monitor the output spiking activity of the I&F neuron. To modulate the DPI’s \( I_g \) gain current we modified the \( V_{\text{thr}} \) bias voltage via an external voltage source, controlled by the same workstation. The voltage \( V_w \) is set by an external voltage reference. To model an average input current produced by the neuron’s full dendritic tree, and used to induce a base activity level, we injected a current \( I_n \) into the neuron’s membrane capacitance. The amplitude of the \( I_n \) current was also controlled by the workstation interfaced to the chip. The sequences of spikes sent to the DPI conversely represent the synapse’s input signal that could drive local spike-based learning circuits.

We carried out experiments analogous to the ones performed on real neurons, simulating the onset of chronic changes in the system: we fixed the statistics of the input spike trains to the DPI and varied the neuron’s input current \( I_n \). The goal of the homeostatic control mechanism is to adapt to these chronic changes on slow time scales, keeping the neuron’s average firing rate close to a set target, and without being affected by fast fluctuations in the neuron’s net input current. The control strategy adopted in our system is that of a classical PI-controller, as shown in Fig. 3: the software algorithm continuously monitors the neuron’s firing rate, in real-time, and determines how to scale the synaptic current by measuring...
fig. 5. Lag compensator control diagram.

the error between the neuron’s firing rate and a target firing rate, and by computing its integral over time. The change in synaptic scaling is then induced by modulating the \( V_{thr} \) bias that acts on \( I_g \).

In Fig.4(b) we show measurements from the HW/SW system for the control case: we combined current injection and synaptic stimulation such that the neuron fired at a desired rate of approximately 98Hz and then produced chronic change in the I&F neuron’s firing rate by applying a step increase in the current \( I_n \). As expected, the PI control algorithm adapted the neuron’s firing rate back to its target value with different time constants depending on the values of \( \tau_H \).

To show that the “slow” homeostatic mechanism does not interfere with “fast” spike-based learning mechanisms we superimposed high-frequency fluctuations to \( I_n \) and repeated the experiment. As shown in Fig.4(b), the DC offset is removed while the high frequency fluctuations are transmitted by the I&F neuron. The amplification of the high-frequency components is due to the choice of the \( K_i \) and \( K_p \) parameters in the control algorithm.

III. ANALOG VLSI IMPLEMENTATION OF THE HOMEOSTATIC CONTROL ALGORITHM

We designed a set of analog circuits to implement the software control algorithm on-chip. Due to the non-idealities of VLSI integrator circuits, we used lag compensation control, shown in Fig.5, instead of pure PI control scheme of Fig.3.

We implemented such scheme with a full-custom analog design using compact low-power (subthreshold) circuits shown in Fig.6. The relationships between the parameters of Fig.5 and the circuit variables are defined as follows:

\[
K_1 = \frac{I_{n_s}}{I_{d_p}} \quad K_2 = \frac{I_{u_a} K_{syn}}{C_s U_T} \quad K_3 = \frac{I_{u_s} I_{g_p} K_{syn}}{C_s U_T}
\]

\[
a = \frac{1}{\tau_i} + \frac{I_{g_i} \kappa_d}{C_s U_T I_{n_p}} \quad b = \frac{1}{\tau_i} \quad c = \frac{1}{\tau} \quad d = \frac{1}{\tau_s},
\]

where the \( \tau \) variables are defined as:

\[
\tau_i = \frac{U_T C_s}{\kappa I_{r_i}} \quad \tau_s = \frac{U_T C_s}{\kappa I_{r_s}} \quad \tau = \frac{U_T C_{syn}}{\kappa I_{r}}
\]

The frequency integration (FI) block consists of a DPI circuit that integrates the output spikes of the I&F neuron into the \( I_{homeo} \) current. The \( I_{error} \) current is generated by comparing the FI block output to the target current \( I_{target} \) set by the constant external bias voltage \( V_{target} \). The integration (INT) block uses another instance of the DPI circuit to integrate the error current over time, producing the \( I_{ie} \) current. The proportional (PROP) block uses a translinear multiplier [18] to multiply the \( I_{error} \) current by constant scaling factors set by \( V_{n_p} \) and \( V_{dp} \), producing the \( I_{pe} \) current.

The control circuit acts on the \( V_{thr} \) bias voltage, which can be connected globally to all DPI synapses afferent to the neuron, to scale their outputs via the \( I_g \) current. The proper value of \( V_{thr} \) is computed on the top right part of the circuit of Fig.6, by summing the \( I_{thr} \), \( I_{pe} \) and \( I_{ie} \) currents.

A. Circuit simulation results

We used TSPICE for circuit simulations. To speed up circuit simulation times, we did not simulate the I&F neuron: assuming that the neuron’s firing is linearly proportional to its input currents, we sourced the sum of \( I_{syn} \) and \( I_n \) in the \( V_s \) node of Fig.6. As for the mixed SW/HW experiments, we fixed \( I_{syn} \) and varied \( I_n \) to model chronic changes and trigger the homeostatic control.

Fig.7(a) shows the transient simulation results for a step decrease in \( I_n \): to compensate for lower net input currents, the
adapt to the chronic change: the control circuit scales $I_n$.(Vzr), thereby compensating for I&F input current change. (b) After the step decrease, the total input current to the I&F neuron is restored by the homeostatic control to a value lying within the control mechanism’s tolerance range.

Fig. 7(b) shows how the neuron’s net input current adapts to the chronic change: the control circuit scales $I_{syn}$ to counteract the effect of the step change in $I_n$.

IV. CONCLUSIONS

Homeostasis is one of the strategies used by biological systems to cope with inhomogeneities and continuous changes of their components while maintaining the capability of learning and adapting to new stimuli. Multiplicative synaptic scaling is a specific type of homeostatic adaptation that has been observed in cultures of cortical, spinal and hippocampal neurons [1], as well as in vivo [19]. In this paper we proposed a possible circuit implementation of the homeostatic synaptic scaling obtained by combining the HW transposition of a lag compensated control algorithm, with a neuromorphic synaptic circuit that supports both Hebbian type of spike-driven plasticity mechanisms as well as global synaptic scaling.

The specific role of homeostatic plasticity mechanisms, with respect to other forms of Hebbian learning is actively being investigated. The proposed circuit, and validated for a single neuron-single synapse system, has been implemented on chips comprising large arrays of silicon neurons and synapses and used as a tool to test different computational theories, in real-time, with real-world stimuli.

In such a system all of the synapses converging to a single neuron will be globally scaled by the proposed circuitry to implement synaptic homeostasis and maintain the activity of each neuron within a functional range, thus counteracting the effect of device mismatch. In addition the new analog homeostatic control circuit designed can be used as a form of global automatic gain control to adapt the system to chronic changes in the input configuration as well as to counteract slow changes in the circuit’s response properties. This mechanism is compatible with conventional engineering solutions for minimizing the effects of mismatch, or compensating temperature drifts, and can be especially useful to compensate for the increasing number of defects expected in the future scaled CMOS processes.

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