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SILICON SYNAPTIC HOMEOSTASIS

Chiara Bartolozzi
Institute for Neuroinformatics
UNI | ETH Zürich
Wintherthurerstr. 190, 8057, Switzerland
chiara@ini.phys.ethz.ch

Giacomo Indiveri
Institute for Neuroinformatics
UNI | ETH Zürich
Wintherthurerstr. 190, 8057, Switzerland
giacomo@ini.phys.ethz.ch

ABSTRACT

Synaptic homeostasis is a mechanism present in biological neural systems used to stabilize the network's activity. It acts by scaling the synaptic weights in order to keep the neurons firing rate within a functional range, in face of chronic changes of their activity level, while preserving the relative differences between individual synapses. In analog VLSI spike based neural networks, homeostasis is an appealing biologically inspired means to solve technological issues such as mismatch, temperature drifts or long lasting dramatic changes in the input activity level. Here we present a new synaptic circuit, the Diff-Pair-Integrator, designed to reproduce the biological temporal evolution of post-synaptic currents, and compatible with implementation of spike-based learning and homeostasis. We describe the silicon synapse and show how it can be used in conjunction with a software control algorithm to model synaptic scaling homeostatic mechanisms.

Keywords:aVLSI; neuromorphic; synapse; homeostasis; spike-based

INTRODUCTION

Learning neural systems are typically faced with two opposing requirements: the need for change and heterogeneity, to adapt to the statistics of the input signals and induce symmetry breaking, and the need for stability and homogeneity, to keep the activity of the neurons within a functional range [1, 2].

In biology these opposing forces are driven by learning mechanisms that induce changes in the weights of individual synapses of the network, acting on time scales ranging from milliseconds to minutes, and by stabilizing homeostatic mechanisms that operate on longer time scales (ranging from minutes to hours) and are not synapse-specific [3].

In recent years much research has been devoted to the construction of biologically inspired pulse-based neural systems, that comprise spike-based learning mechanisms [4, 5, 6, 7]. Many of the learning algorithms and circuits proposed avoid uncontrolled increase of synaptic weights and keep the system's activity within functional boundaries. However few VLSI pulse-based neural systems have been explicitly designed to implement homeostatic plasticity stabilizing mechanisms [8]. VLSI models of homeostatic plasticity can be used as additional strategies to cope with fluctuations induced by temperature changes, drift, or device mismatch effects. In addition, in large multi-chip VLSI implementations of neural systems [9] instabilities could arise also due to dramatic changes in the statistics of the input signals, induced for example by the incorporation of new input devices, by failures in existing sensory input devices, or by abrupt changes in the testing environment. In these situations the addition of silicon homeostatic mechanisms could lead to improvements in the overall system performance and stability.

Several types of stabilizing homeostatic mechanisms have been revealed in neurophysiology (see [1] for a detailed review). The specific mechanism we address in this work is referred to as *activity-dependent scaling of synaptic weights* [3]. This process acts by globally scaling the weights of the entire distribution of synapses afferent onto one postsynaptic neuron, in response to chronic alteration of its output firing activity. The multiplicative nature of this mechanism preserves the relative differences between synaptic weights acquired by learning. This type of

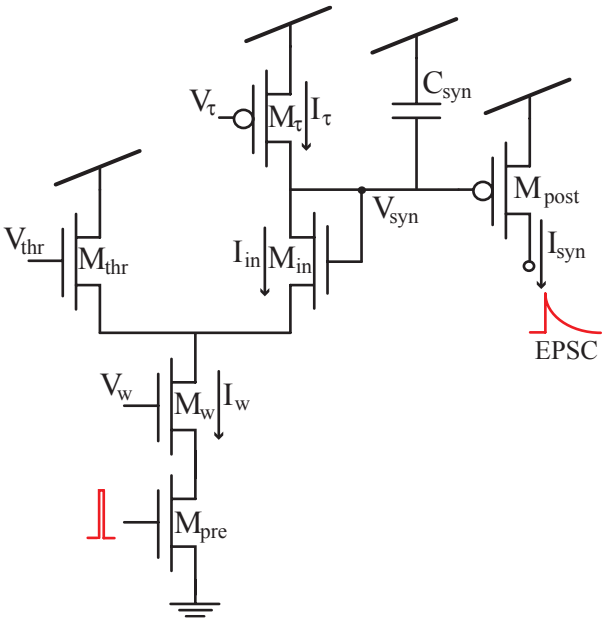

Figure 1. Diff-pair integrator synapse: The circuit comprises 4 n-FETs, 2 p-FETs and one capacitor. The n-FETS implement a differential pair, the M_τ p-FET acts as a constant current source, while the M_{post} p-FET injects the output current I_{syn} into the membrane capacitor of the target I&F neuron (not shown). When an input pulse reaches M_{pre}, I_w starts to flow through M_w, and the current $I_{in} - I_\tau$ discharges the capacitor C_{syn}, decreasing the voltage V_{syn}; this results in an exponential increase of the output current I_{syn}. As soon as the input pulse ends M_{in} switches off and the transistor M_τ charges the capacitor C_{syn} linearly; this results in an exponential decrease of I_{syn} with time.

homeostatic plasticity has been shown to exist both in cultures of neurons and *in vivo*, during development. Together with the complementary spike-based learning mechanisms, the synaptic scaling homeostatic mechanism forms an ensemble of strategies for the control of the network's overall stability.

In this paper we present a VLSI synaptic circuit, the Diff-Pair Integrator, that supports both spike-based learning rules and homeostatic synaptic scaling. To demonstrate the stabilizing properties of homeostatic control, we implemented homeostasis as a software control system, in loop with a chip comprising a VLSI implementation of the synapse. We show experimental data from the mixed-mode SW/HW neural system, and propose analog circuits for designing a full custom analog VLSI implementation of the homeostatic control algorithm.

THE DIFF-PAIR INTEGRATOR SYNAPSE

The Diff-Pair Integrator (DPI) circuit implements a log-domain filter that reproduces the exponential dynamics observed in excitatory and inhibitory postsynaptic currents (EPSCs and IPSCs respectively) of biological synapses [10]. The circuit we propose has the useful property of being a *linear* integrator, with independent control of time constant, synaptic weight, and synaptic scaling parameters. The circuit's schematic diagram is shown in Fig.1.

We can demonstrate analytically that the circuit's behaves as a linear filter, when it is operated in the subthreshold regime [11]. In this regime, and making the realistic assumption that the transistors are saturated, we can write:

$$I_{in} = I_w \frac{e^{\frac{\kappa V_{syn}}{U_T}}}{e^{\frac{\kappa V_{syn}}{U_T}} + e^{\frac{\kappa V_{thr}}{U_T}}} \tag{1}$$

$$I_c = C_{syn} \frac{d}{dt}(V_{dd} - V_{syn}) \tag{2}$$

$$I_{syn} = I_0 e^{\frac{\kappa(V_{dd} - V_{syn})}{U_T}} \tag{3}$$

where I_0 is the leakage current, κ is the subthreshold slope factor [11], and U_T is the thermal voltage.

Taking into account that $I_c = I_{in} - I_\tau$ and that $\frac{dI_{syn}}{dt} = -\frac{\kappa}{U_T} I_{syn} \frac{dV_{syn}}{dt}$, we can combine all equations above to obtain:

$$\tau \frac{dI_{syn}}{dt} = -I_{syn} + \frac{I_w}{I_\tau} \frac{I_{syn}}{1 + \left(\frac{I_{syn}}{I_{thr}}\right)} \tag{4}$$

where $\tau = \frac{C U_T}{\kappa I_\tau}$ is the circuit's time constant and the term $I_{thr} = I_0 e^{\frac{\kappa(V_{dd} - V_{thr})}{U_T}}$ represents a virtual p-type subthreshold current that is not tied to any p-FET in the circuit.

If we apply an input step to M_{pre}, the output current I_{syn} rises monotonically. As soon an $\frac{I_{syn}}{I_{thr}} \gg 1$ the non-linear differential equation reduces to a first order linear differential equation, with the following step-response:

$$I_{syn}(t) = \frac{I_w I_{thr}}{I_\tau} \left(1 - e^{-t/\tau}\right) \tag{5}$$

assuming $I_{syn}(0) = 0$ as initial condition.

Silicon synapses are typically stimulated with trains of pulses (spikes) of very brief duration, separated by longer inter-spike intervals (ISIs). During the inter-spike-interval the output current decays exponentially with the profile

$$I_{syn}(t) = I_{syn}(t_n^+) e^{-\frac{(t - t_n)}{\tau}} \tag{6}$$

where $I_{syn}(t_n^+)$ is the residual output current at the end of the n^{th} spike.

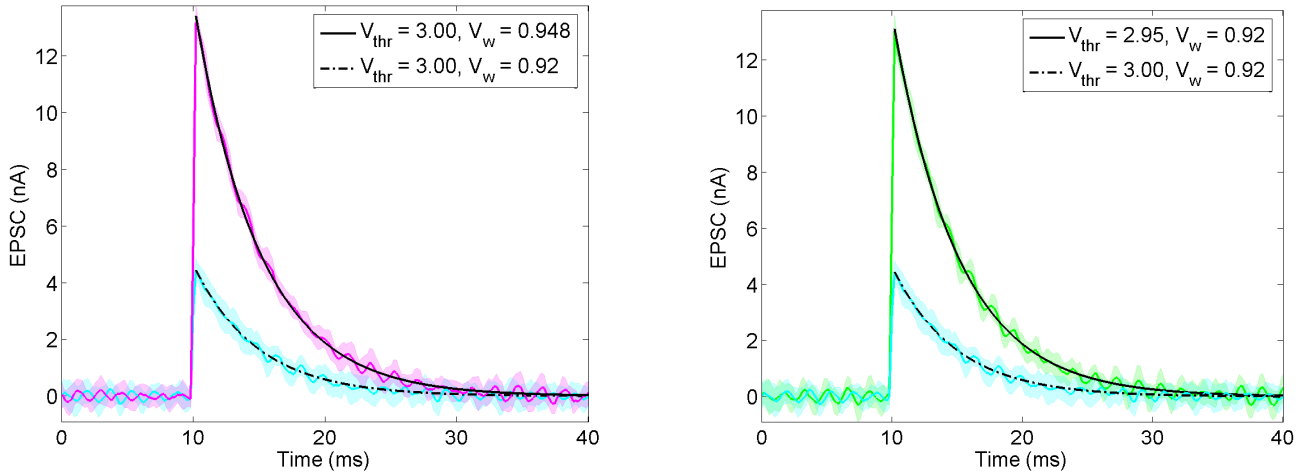

Figure 2. The amplitude of the EPSC generated by the DPI can be independently adjusted with V_{thr} and V_w: The plots show the time course of mean and standard deviation (over 10 repetitions of the same experiment) of the current I_{syn}, in response to a single input voltage pulse. In both plots the lower EPSC traces share the same set of V_{thr} and V_w, in (a) the higher EPSC is obtained by increasing V_w while in (b) by decreasing V_{thr}, with respect to the initial bias set. Superimposed to the experimental data we plot theoretical fits of the decay from Eq. 6. The time constant obtained from the fits of all the three different EPSCs is $5ms$, confirming the findings of our analytical solution that changing the synaptic weight with any of the two parameters does not change the kinetics of the current.

The time constant of the EPSC can be set by tuning V_τ of Fig. 1. Once the EPSC's kinetics is set, its maximum amplitude can be controlled by independently adjusting the synaptic weight V_w and/or the diff-pair threshold V_{thr}. In Fig. 2 we show this property with data obtained from a test DPI circuit, implemented in VLSI using a standard CMOS 0.35μ technology, in which we instrumented the output current.

At steady-state, when stimulated with a spike train of average frequency f_{in}, the mean EPSC is:

$$< I_{syn} >= \left(\frac{I_{thr} I_w}{I_\tau} \right) \tau f_{in} \tag{7}$$

The total gain of the synapse can be therefore set by varying both I_w and I_{thr} (see also Fig. 2). We exploit these two independent degrees of freedom for learning the synaptic weight V_w with "fast" spike-based learning rules, while slowly adapting the bias V_{thr} to implement homeostatic synaptic scaling.

EXPERIMENTAL SETUP AND HOMEOSTATIC CONTROL ALGORITHM

In our setup we used a DPI synapse connected to a low power adaptive Integrate and Fire (I&F) neuron [12]. Both circuits were integrated in a custom VLSI chip. The chip was implemented using a standard 0.5μm technology and fabricated through the MOSIS consortium.

We connected the chip to a linux desktop to monitor the spiking activity of the I&F neuron in real-time, and to send sequences of spikes to the synapse [13]. The desktop is also used to control a current source that injects a current I_n to the input capacitance of the I&F neuron, and to control a voltage source that sets the value of the DPI's V_{thr} bias voltage (see Fig. 1).

In our experiments we stimulate the neuron using both current injection (sourced into the neuron's capacitance) and spike trains (sent to the DPI). The current I_n models the average input current that the neuron would receive from its full dendritic tree, and is used to induce a base activity level. The sequences of spikes conversely represent the synapse's input signal, and could drive a spike-based learning circuit, such as the one proposed in [7], or in [14].

To characterize our synaptic homeostasis model we fix the statistics of the synapse input spike trains and vary the neuron's input current I_n. The homeostatic control algorithm then adapts the DPI's V_{thr} bias to maintain the neuron's output firing rate within a desired (functional) range. Formally, the control strategy adopted is that of a PI-controller: The algorithm determines how to change V_{thr} both by measuring the error between the neuron's firing rate and its target firing rate, and by computing its integral over time. The block diagram of this classic control system is shown in Fig. 4.

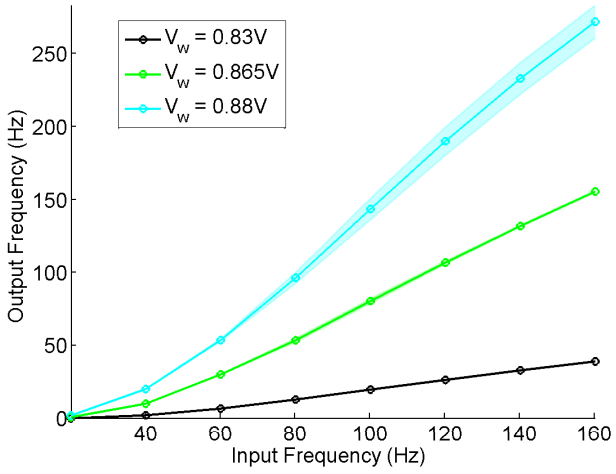

Figure 3. Firing rates mean and standard deviation (over 10 repetitions of the same experiment) of the I&F neuron when its input synapse is stimulated with regular spike trains, for different values of V_w. The measures are consistent with our mathematical analysis: the output frequency is linear with the mean current injected by the synapse (Eq. 8), the current is in turn linear with the synaptic input frequency (Eq. 7).

The system of differential equations that implements this control strategy is:

$$\begin{cases} \tau_H \dot{f}(t) = -f(t) + f_i \\ f_i = \alpha(I_n(t) + I_{syn}(t)) \\ e(t) = (f_t - f(t)) \\ I_{syn}(t) = k_p e(t) + k_i \int_0^t e(\xi) d\xi \end{cases} \quad (8)$$

where τ_H is the time constant of the homeostatic process, f_i is the neuron's measured instantaneous firing rate, α is the neuron's transfer function gain, when the neuron is operating in its linear region [12], f is the neuron's integrated firing rate, and f_t is a desired target firing rate.

This control algorithm determines the value of I_{syn} required to keep the neuron's firing rate close a defined target rate; the updated value of I_{syn} depends proportionally on the distance between them, the error $e(t)$, and on its integral over time, with the proportionality constants k_p and k_i respectively. To set I_{syn} to the new desired value, we use Eq. 7 and modify I_{thr} (via V_{thr}) accordingly.

This software algorithm can be directly mapped on silicon: another instance of the DPI circuit can be used to implement the integration over time of the post-synaptic neuron's output firing rate, a differential pair can be used to realize the proportional control, and a follower integrator circuit can be used to implement the integral control.

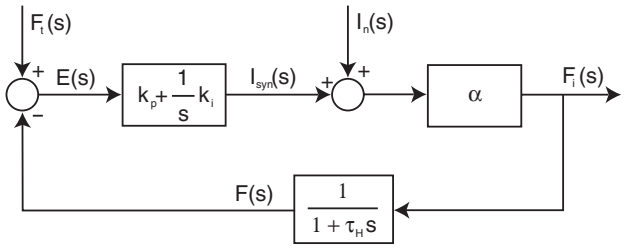

Figure 4. Block diagram of the discrete homeostatic control PI algorithm, in the Laplace domain. $I_n(s)$, the disturbance input, and $I_{syn}(s)$, the system's controlled variable, are the current inputs to the I&F neuron. The feedback block integrates the neuron's output frequency $F_i(s)$ over time, the resulting low-pass filtered frequency $F(s)$ is then compared to the target frequency $F_t(s)$, generating the error $E(s)$ that drives the PI-controller block. It sets the controlled signal I_{syn} to a value that brings the neuron's output firing rate back to the reference value $F_t(s)$.

EXPERIMENTAL RESULTS

To demonstrate the properties of our homeostatic control setup, we replicated the experiment described by Turrigiano and colleagues [3], where they chronically shifted the activity of the neurons to uncover the synaptic scaling behavior. Specifically, we initially combined current injection and synaptic stimulation such that the neuron fired at a desired rate of approximately 98Hz. Subsequently we produced a step change in the I&F neuron's firing rate by changing the injection current I_n, and let the control algorithm scale the total synaptic efficacy. As shown in Fig. 5, the homeostatic control adapted the neuron's firing rate back to its target value with a time constant τ_H. In the experiment shown in Fig.5, the control algorithm adapted the V_{thr} bias from a value of $4.5V$ to one of $4.58V$. This produced a decrease of I_{thr}, that in turn scaled the EPSC's amplitude proportionally, reproducing the behavior observed in [3].

Ideally the (slow) homeostatic stabilizing mechanism should not interfere with the (fast) spike-based learning mechanisms. To show that our homeostatic control algorithm corrects only chronic DC shifts of activity, letting the information associated with the fast fluctuations of the input signal pass through, we superimposed high-frequency fluctuations to I_n and repeated the chronic (step) change experiment. Fig. 6 shows the results of this experiment. As shown, DC offset is removed while the high frequency fluctuations are transmitted by the I&F neuron. The amplification of the high-frequency components is due to the choice of the k_i, and k_p parameters in the control algorithm.

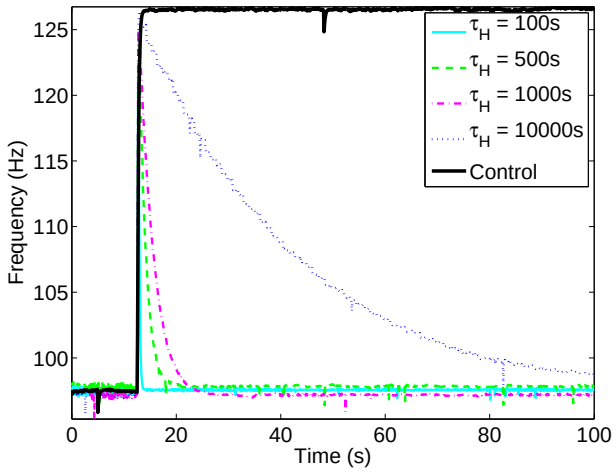

Figure 5. Homeostatic response to a step-wise DC shift in the neuron's instantaneous firing rate. The thick black line shows the output of the neuron for a step in the input current level when the homeostatic control is not enabled. The other curves show how the firing rate goes back to the initial activity level for different time constant of the homeostatic control.

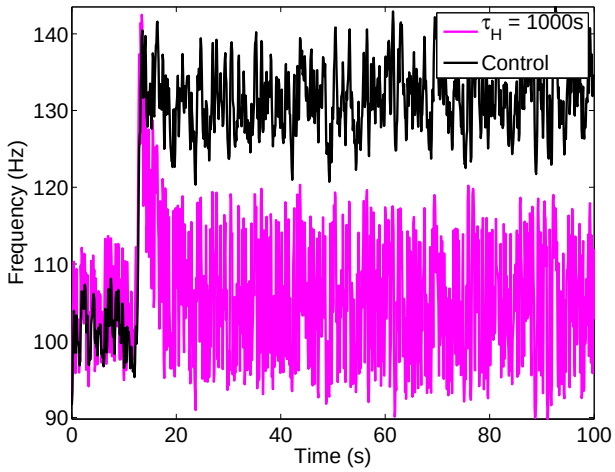

Figure 6. Homeostatic control adding high frequency fluctuations to the injection current: we replicate the same experiment of Fig. 5, adding random noise, for the time constant $\tau_H = 1000s$; the black line shows the output of the neuron for a step in the input current level when the homeostatic control is not enabled. The blue curve shows how the DC offset in the firing rate is corrected, without affecting the high frequencies.

CONCLUSIONS

Multiplicative synaptic scaling has been shown in cultures of cortical, spinal and hippocampal neurons [15], and has been shown to exist also *in vivo* [16]. The specific role of this particular type of homeostatic plasticity mechanism, with respect to other forms for stabilization in Hebbian forms of learning is still debated. We can however use this biologically inspired mechanism as an additional strategy used to solve some technological issues raised by the physical implementation of neural networks in silicon, such as drift, temperature dependence, and mismatch.

We proposed a new silicon synapse circuit (the DPI) that supports both spike-based learning rules [7, 14] and homeostatic plasticity, thanks to its extra degree of freedom provideded by V_{thr}, independent from the synaptic time constant and weight V_w. In networks of spiking neurons this circuit allows to scale the output current of all synapses converging on each single neuron, by connecting their V_{thr} node to the same bias. This multiplicative form of synaptic scaling preserves the individual learnt weights and the relative differences among synapses.

In large aVLSI networks of spiking neurons [7] we can therefore act on all synapses of each neuron to maintain their activities within a functional range: this will naturally adapt out inhomogeneities across neurons caused by mismatch. At the network level, this homeostatic mechanism counteracts the effect of temperature drifts that can change the spiking activity of the neurons; at the system level this mechanism acts as an automatic gain control that responds to dramatic changes in input activity levels, i.e. when an operating chip is interfaced to a new sensory input device.

The on-line homeostatic plasticity mechanism was modeled using dedicated HW [17] and SW [13] tools for communicating in real time with analog asynchronous spiking devices. We demonstrated the stabilizing properties of the homeostatic control algorithm, and argued that such type of homeostatic control strategies can compensate for inhomogeneities in the network, to slow drifts in overall network activity, or to dramatic changes in network inputs.

In the long-term we plan to investigate implementation of the control algorithm described in this paper directly in VLSI, potentially using floating gate devices to achieve the long time constants required in order to avoid interference with faster adaptation and learning mechanisms present in the silicon synapses and neurons.

ACKNOWLEDGMENTS

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Giacomo Indiveri is a Research Assistant at the Institute of Neuroinformatics of the Swiss Federal Institute and the University of Zurich. He obtained his master degree in electrical engineering from the University of Genoa, Italy in 1992 and won a post-graduate fellowship within the "National Research Program on Bioelectronic technologies" from which he graduated (*cum laude*) in 1995. From 1994 to 1996 he worked as a Postdoctoral fellow in the Dept. Biology at the California Institute of Technology, on the design of analog VLSI neuromorphic devices for low-level visual tasks and motion detection. His current research interests include the design and implementation of neuromorphic systems for modeling selective attention neural mechanisms, and for exploring the computational properties of networks of silicon integrate and fire neurons. Dr. Indiveri is co-teacher of two classes on the analysis and design of analog VLSI Neuromorphic Systems at the Swiss Federal Institute of Zurich, co-organizer of the Workshop on Neuromorphic Engineering, held annually in Telluride, and co- author of the book *"Analog VLSI, Circuits and principles"*, by Liu et al. from MIT Press.

Chiara Bartolozzi was born in Genoa, Italy in 1977. She received the Laurea degree in biomedical engineering from the University of Genoa (*cum laude*) in 2001. Currently she is pursuing her Ph.D. degree at the Institute for Neuroinformatics, UNI/ETH Zurich, Switzerland. Her research interests are mainly directed toward design and implementation of neuromorphic analog VLSI models of selective attention.