

# A low-power dual-threshold comparator for neuromorphic systems

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## Abstract

Neuromorphic systems typically use VLSI circuits and devices that implement models of biological systems for processing sensory signals. The analog circuits used in neuromorphic systems operate on signals that change slowly in time, with biological time-constants of the orders of milliseconds, and are characterized by very low-power consumption. Here we present a low-power circuit, with small slew-rate, that can be used as a building block in neuromorphic systems for dual threshold comparison. The circuit is compact, operates in weak-inversion, and dissipates power only when the input signal is within a required range.

## 1 Introduction

Neuromorphic systems are hardware devices, containing analog circuits, that attempt to model in detail, (down to the device-physics level) the properties of biological systems and the physical processes in them embedded that underlie neural computation [2]. Using analog, continuous-time circuits implemented with a standard CMOS VLSI technology it is possible to build compact implementations of such models. As these systems typically contain large arrays of basic processing elements operating in a massively parallel fashion, the circuits used should consume very low-power. On the other hand, given the time-constants of the signals typically used in neuromorphic systems, speed requirements are usually less stringent. Here we propose a novel dual-threshold comparator circuit used for comparing a signal between two independent thresholds. The circuit has been designed to implement comparator blocks in learning networks of integrate and fire neurons [1], but it can also be useful for other applications, such as smart sensors or prosthetic devices. Making a very compact low power circuit that can be repeated in

a densely packed neuromorphic VLSI array is a major motivation for this design.

## 2 The dual threshold comparator

Detecting the existence of a signal between two independent thresholds can be easily achieved with two standard comparators and a digital 'AND' gate. This would typically require 15 to 20 Field-Effect-Transistors (FETs) and significant amount of DC power consumption. If the speed requirements are not very stringent, the same functionality can be achieved with more efficient and compact circuits: the circuit we propose requires only 8 MOS-FETs, and dissipates very small amounts of current, only when the signal is within the two thresholds.

### 2.1 Circuit concept

To reduce power consumption we designed our circuit to operate in the weak-inversion, or subthreshold domain. The current-voltage relationship of an n-FET in this domain is given by,

$$I_{ds} = I_{0n} e^{(\kappa_n V_g - V_s)/U_T} (1 - e^{-(V_d - V_s)})$$

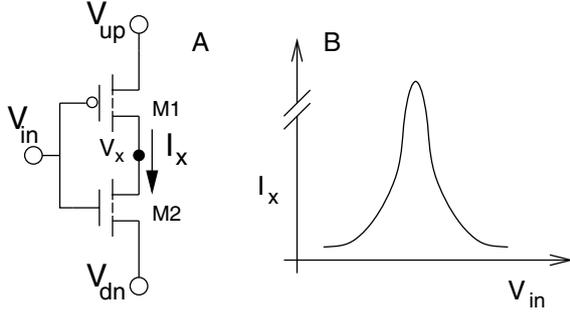
where  $I_{0n}$  is the specific current [4],  $\kappa_n$  is the subthreshold slope coefficient for n-FET, and  $U_T$  is the thermal voltage [3].

In the subthreshold domain if  $V_d - V_s > 4U_T$  (*i.e.*  $V_{ds} > 100mV$  at room temperature) the transistor is in saturation and the above equation simplifies to:

$$I_{ds} \approx I_0 e^{(\kappa_n V_g - V_s)/U_T}$$

In this condition one can use a single n-FET to compare the difference between two voltages (modulo the  $\kappa_n$  factor). If the difference is positive the n-FET will sink a current  $I_{ds} > I_0$ . The output current generated is not a crisp function of the input difference (due to it's

\*This work is supported by the EU ALAVLSI grant (IST-2001-38099), and by the ETH TH-Project 0-20174-04.



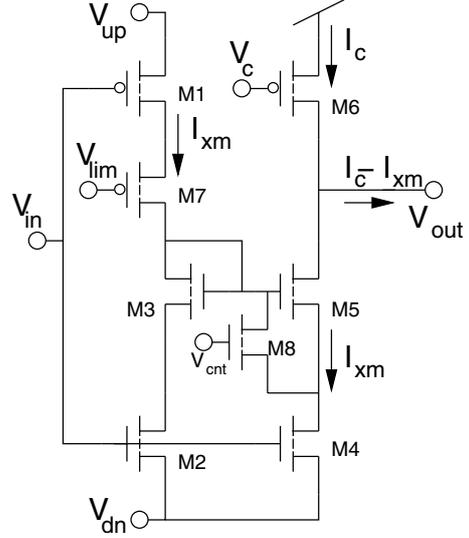
**Figure 1:** Dual threshold comparison circuits. (A) Basic N-P configuration (described in the text) (B) Output current of the basic comparator  $I_x$  as a function of the input voltage  $V_{in}$ .

exponential nature), but can be used to compare slowly varying signals.

We can analyze the characteristics of a dual comparator based on this principle by considering two complementary MOSFETs connected with common gate voltage as in Fig. 1A. The circuit essentially consists of two independent current sources in series. As the input voltage  $V_{in}$  increases linearly, the branch current  $I_x$  has an initial exponential increase, and is followed by an exponential decrease, as sketched in Fig. 1B. The smaller of the two current-sources in series, determines the steady state branch current  $I_x$ . As in an inverter, non-negligible current is generated only when the gate voltage lies within the two source voltages ( $V_{up}$  and  $V_{dn}$ ). The peak value of  $I_x$  is given by  $I_0 e^{(V_{up}-V_{dn})/U_T}$ , assuming the specific current and subthreshold slope factors are the same for n- and p-FETs ( $\kappa_n = \kappa_p$ ,  $I_{0p} = I_{0n} = I_0$ ). The drain currents of a p- and n-FET are shown in logarithmic axis in Fig. 3 (dotted lines) along with  $I_x$  (solid line). As  $I_x$  is always in subthreshold the plot takes a triangular shape, on a log scale.

As the input voltage  $V_{in}$  increases, the voltage at  $V_x$  switches from  $V_{up}$  to  $V_{dn}$ . This ensures that either M1 or M2 are always in saturation. The dominant current source being always in saturation validates the previous approximations for  $I_{ds}$ .

The full dual-comparator circuit we propose is shown in Fig. 2. The circuit consists of two complementary MOSFETs, similar to that of Fig. 1A (M1 and M2), and six additional MOSFETs for further processing: the n-FETs M2 through M5 are used to mirror the current  $I_x$  to the output branch. The n-FETs M2 and M4 have the same  $V_{gs}$  and operate in saturation for most of the circuit's operating range. This ensures that also M3 and M5 have similar source voltages, hence the current mirror produces a faithful copy of the input current  $I_x$ :  $I_{xm}$ . For high values of  $V_{in}$ , M2 and M4 enter the ohmic



**Figure 2:** Full dual threshold comparator circuit: the input voltage  $V_{in}$  is compared to two signals set by  $V_{dn}$  and  $V_{up}$ . The output voltage  $V_{out}$  is low ( $V_{out} = V_{dn}$ ) when  $V_{in}$  is within this range and high  $V_{out} = V_{dd}$  otherwise.

region of operation, causing slight mismatch in the mirroring operation. The copy of  $I_x$ ,  $I_{xm}$ , is subtracted from a constant current  $I_c$ . The resulting current flowing out of the output node  $V_{out}$  is  $I_c - I_{xm}$ . The output voltage  $V_{out}$  switches between  $V_{dd}$  and  $V_{dn}$  as  $I_c - I_{xm}$  changes sign. In this scenario, the pull up transistor M6 (carrying  $I_c$ ) determines the speed at which  $V_{out}$  can change from  $V_{dn}$  to  $V_{dd}$ . The condition  $I_x = I_c$  is satisfied for two values of  $V_{in}$ . To first order approximation, these values are:

$$V_{dn}^t \triangleq \frac{1}{\kappa} \left( U_T \ln \frac{I_c}{I_{0n}} + V_{dn} \right) \quad (1)$$

$$V_{up}^t \triangleq \left( V_{up} - U_T \ln \frac{I_c}{I_{0n}} \right) \quad (2)$$

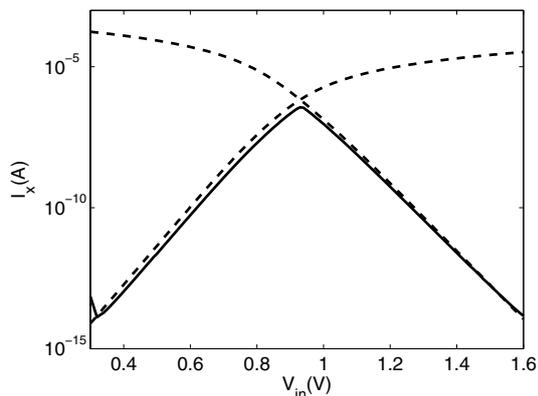
Taking into account that  $I_c = I_{0p} \exp^{\kappa(V_{dd}-V_c)/U_T}$  and assuming  $I_{0n}=I_{0p}$  the above equations can be further simplified to;

$$V_{dn}^t = (V_{dd} - V_c) + \frac{V_{dn}}{\kappa}$$

$$V_{up}^t = V_{up} - (V_{dd} - V_c)$$

The above equations provide us with two simple expressions for  $V_{dn}$  and  $V_{up}$  that should be used to determine the desired switching point.

If  $V_{up}$  and  $V_{dn}$  differ by large amounts the peak current  $I_x$  can reach very high values, and the transistors can enter the strong inversion regime. To reduce the



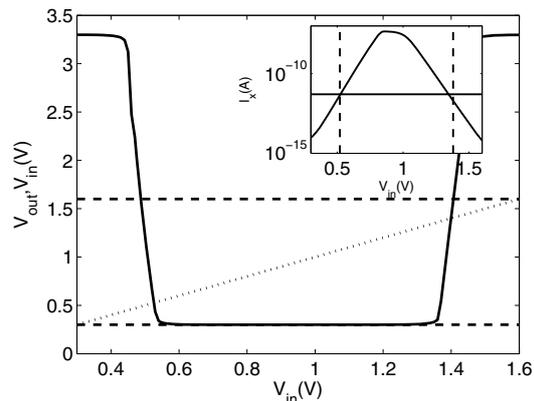
**Figure 3:** Log plots of drain currents for individual p- and n-FET as a function of  $V_{gs}$  (dotted lines) and the effect of combining them on one branch (solid line).  $V_{up}$  and  $V_{dn}$  are set to 1.6V and 0.3V respectively.

maximum current dissipation and keep the transistors in the weak-inversion regime we used an additional n-FET (M7) biased with an appropriate constant voltage  $V_{lim}$ . Finally, the comparator can be shut off completely and activated only when required by using the n-FET M8 with the control signal  $V_{cnt}$ . If  $V_{cnt}$  is high, the current in the mirror M3,M5 is switched off (by shorting the  $V_{gs}$  of M5), thus allowing M6 to pull the output node  $V_{out}$  high, eventually bringing M6 into the triode region of operation and switching it off.

## 2.2 Simulation results

The circuit was simulated with Tanner Spice for  $0.35\mu\text{m}$  AMS process parameters. The circuit's response to a linearly increasing input signal is shown in Fig. 4. As shown, the output voltage initially switches from high to low, when the input voltage crosses the first threshold  $V_{dn}^t$ , and subsequently goes back high, as  $V_{in}$  crosses  $V_{up}^t$ . The inset of Fig.4 shows the current-limited branch current  $I_x$  as a function of  $V_{in}$ . The dashed lines in the inset represent the values of  $V_{dn}^t$  and  $V_{up}^t$  as computed by eq.(2). As shown, these estimated values are close to the intersection of the measured  $I_c$  with  $I_x$ . To obtain the rail-to-rail output swing shown in Fig.4, the current  $I_c - I_{xm}$  was mirrored by an additional p-FET and compared to an n-FET current-source with source tied to ground. This additional stage does not increase the power dissipation by a significant amount, and changes the polarity of the output voltage. The circuit's slew rate, in open loop mode, is approximately  $10\text{V}/\mu\text{s}$ .

Simulation also confirm that the addition of the n-



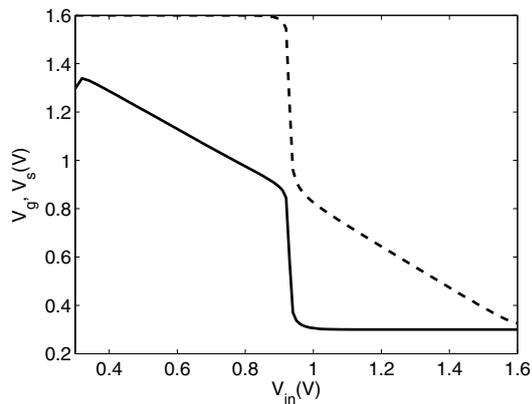
**Figure 4:** Simulation results for a linearly increasing input voltage and the switching output (solid line). The dashed lines shows  $V_{dn}$  and  $V_{up}$ .  $I_x$  with its peak value limited by M7 Fig.1 is shown in the inset along with comparing current  $I_c$ . Theoretically calculated  $V_{dn}^t$  and  $V_{up}^t$  are shown by dashed lines.

FET M3 doesn't change the shape of  $I_x$  and its dependence from  $V_{in}$ , as in the circuit of Fig. 1A. In Fig.5 we show how the  $V_{gs}$  of M3 changes to accommodate the changes in  $I_x$ : the gate voltage of M3 is plotted with a dashed line (top trace), while its source voltage is plotted with a solid line (bottom trace).

For input voltages that lie outside the thresholds ( $V_{in} < V_{dn}$ ,  $V_{in} > V_{up}$ ), the only amount of current dissipated is due to leakage currents. This ensures minimal power consumption for a large region of operation (0 to  $V_{dd}$ ). While the signal is in between the thresholds the power consumption is minimized by limiting the current in left branch with n-FET M7 and by using a subthreshold current-source M6 on the output branch. In the circuit simulations used for the data of Fig.4 the maximum power dissipation was lower than  $10\text{nW}$ . In typical operating conditions a full rail-to-rail swing of  $V_{out}$  is obtained by setting the constant current  $I_c$  to approximately 100 times the specific-current ( $I_0$ ), and the maximum  $I_x$  current to approximately 100 times  $I_c$ . We implemented the circuit using a  $0.35\mu\text{m}$  AMS CMOS process. In this process the dual-threshold comparator circuit occupies an area of approximately  $300\mu\text{m}^2$ .

## 3 Conclusions

We presented a compact dual-threshold comparator circuit, that uses fewer components than equivalent circuits designed using conventional approaches. This dual-threshold comparator has extremely low-power



**Figure 5:** Gate voltage trace (dashed line) and source voltage trace (solid line) of n-FET M3, as a function of input voltage. Both voltages change to accommodate the branch current  $I_X$ .

consumption characteristics. The low slew rate of the circuit makes it suitable for use in neuromorphic systems, and in application in which the input signal changes slowly in time. The fact that the comparator doesn't dissipate power when input signal is out of range, makes it a useful circuit block for massively parallel systems that require dense architectures with such computational capability.

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