

# An aVLSI Basis for Dendritic Adaptation

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**Abstract**—We have developed and described an analog electronic circuit that adapts the electrotonic properties of a silicon dendrite. The dendrite is modeled by the method of compartmental modeling, consisting of three dendritic compartments each containing a synaptic conductance, and one somatic compartment containing a spiking mechanism. Dendritic synaptic input is represented as an activity signal, which scales the leakage conductance of the dendrite. This adaptive feedback loop ensures a controlled synaptic integration in the dendrite, and so regulates the somatic firing frequency. The general adaptive mechanism can therefore be used for building highly dynamic neural networks.

**Index Terms**—Adaptation, dendrite, short-term.

## I. INTRODUCTION

EXPERIMENTAL and theoretical studies suggest that neurons continuously regulate their own I/O relation. The regulation seems to occur at all functional levels—soma, synapse, dendrite—and on different time scales—milliseconds to hours and days. At the *somatic* level, there exists “spike frequency adaptation,” the phenomenon of increasing inter-spike interval length, in response to a sustained step current [1], [2]. A similar form of adaptation also seems to take place at the long-term scale: the neuron changes its I/O relation to adapt to its own input [3]–[6]. At the *synaptic* level, it is the synaptic strength that changes on a short- and long-term scale [1]. In response to a presynaptic spike, the synaptic strength can either increase or decrease. While the long-term changes (long-term depression and potentiation) are associated with learning of synaptic weights in a network, the short-term changes like synaptic depression and facilitation are associated with for example cortical gain control [7], [8]. Finally, at the *dendritic* level, there is evidence for adaptation as well. Ionic conductances in the dendrite can change according to the synaptic activity and so influence electrotonic spread in dendrites [9], [10]. Although modeling this dendritic mechanism has been less popular in network approaches, modelers have now also attacked this form of regulation [11]. All these forms of adaptation at various functional levels and time scales are presumably important for a balanced operation of neurons in a network with continuously changing inputs.

Neuromorphic engineers try to replicate this flexibility by building neurons that adapt their I/O function to changes in their input as real neurons do (see discussion for implemented ex-

amples). Here we report on an analog circuit executing adaptation of electrotonic spread in a silicon dendrite. Dendrites are modeled by the method of compartmental modeling [12]. The idea of this method is to discretize the dendrite into equivalent, connected cylinders of dendritic membrane, so-called compartments [Fig. 1(a)]. Each compartment contains a *RC* circuit, which represents the electrical passive behavior of that piece of membrane. The compartments are serially connected by axial (or horizontal) resistors, which emulate the axial resistance (or internal resistance) of the dendritic cable. In engineering terms this circuit is called a *RC*-delay line. We have constructed such a dendrite in aVLSI and we report on this in detail elsewhere [13]. In this work we change the leakage conductance of each compartment by an activity signal, which represents the synaptic activity of the entire dendrite. Such modulation of the leakage conductance influences the electrotonic spread of synaptic propagation and therefore its integration in the dendrite.

## II. METHODS

Our dendritic *RC*-delay line is a mixture of Elias’ and our method of simulating resistors: The compartmental *RC* circuit is approximated by a follower integrator, whose (fixed, positive) input is the resting potential of the neuron [13]; the axial resistance is simulated by Elias’ switched-capacitor method [14]. Each compartment contains an excitatory synaptic conductance [shown in Fig. 1(b) in equivalent electrical form]. We feed these synaptic circuits with presynaptic pulses (SPK) of 1–ms width, which generate a synaptic current that lasts about 2–3 ms (details in [15]). The basic operating principles of the dendrite (excitatory post-synaptic potential propagation and effects of different parameter values) will be reviewed in Fig. 2. As a somatic spiking mechanism we use a previously constructed set of somatic ionic conductances, that is the sodium and the potassium conductance [16], [17]. More details on our silicon dendrite are given in [13].

The adaptation algorithm operates in three steps [Fig. 1(c)]: Firstly, creation of an activity signal,  $V_{si}$ , which is proportional to the frequency of all synaptic input [see dotted arrows pointing from Fig. 1(b) to (c)]; secondly, low-pass filtering of  $V_{si}$ , yielding what we call the activity sensor,  $V_{se}$ ; thirdly, comparison of  $V_{se}$  to a reference voltage, SEREF, which determines the magnitude of the leakage conductance [see dashed arrows pointing from Fig. 1(c) to (b)].

*Step 1:* The creation of  $V_{si}$  is analogous to the creation of the activity signal for spike frequency adaptation and synaptic depression [18] and [18], for each signal. In our case a presynaptic spike SPK, a fixed amount of current,  $I_{in}$ , is dropped onto  $C_{si}$ . SPK is thus used twice, for triggering the synaptic circuit as well as the adaptation circuit.  $I_{in}$  is generated by transistors, T1x and T2, and a current mirror, CM1. For each synapse (x) there is a

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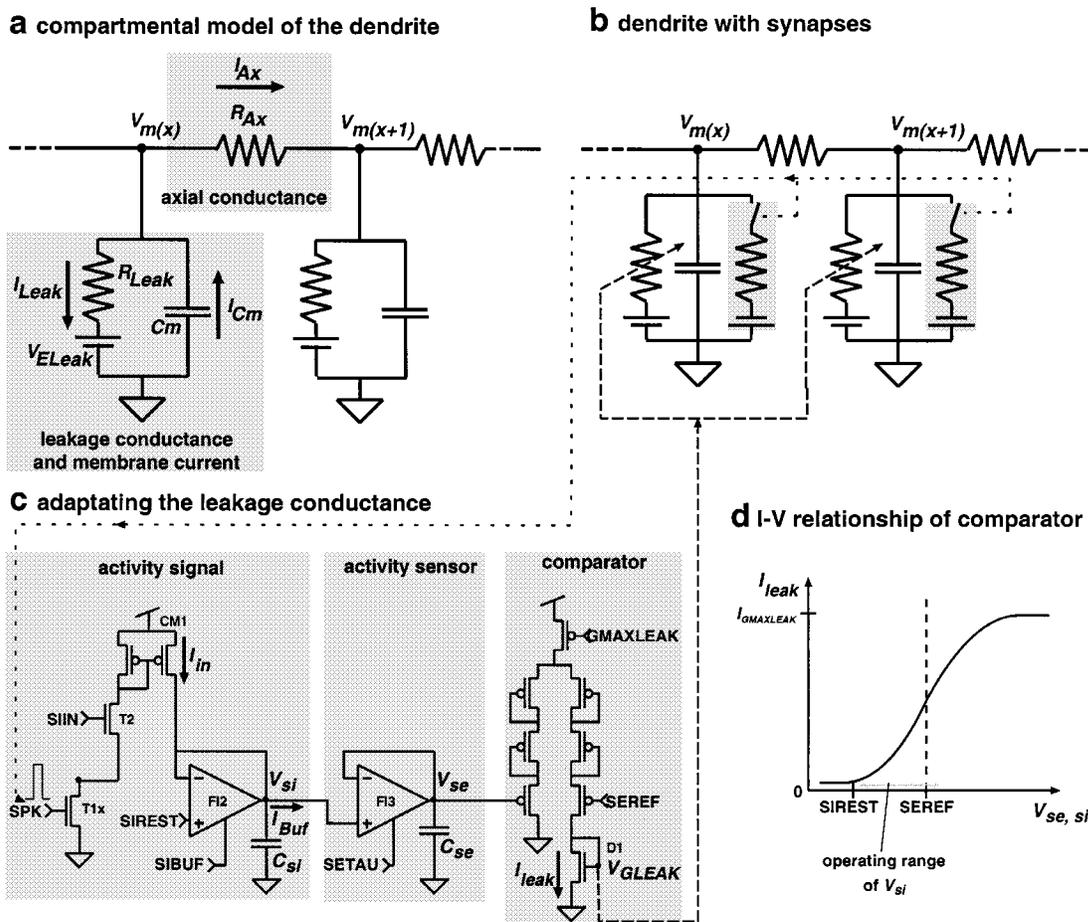


Fig. 1. Adaptive dendritic circuits. (a) Electrical diagram of a compartmental model of a piece of dendrite:  $RC$  circuits (leakage conductance and membrane current) are connected by axial conductances.  $C_m$  represents the membrane capacitance.  $R_{Leak}$  simulates the membrane resistance, through which current ( $I_{Leak}$ ) leaks away.  $V_{ELeak}$  represents the resting potential of the entire neuron.  $V_{m(x)}$  and  $V_{m(x+1)}$ , represent the membrane potentials in compartments  $x$  and  $x + 1$ , respectively.  $R_{Ax}$  simulates the axial resistance. (c) Each of the dendritic compartments contains a synaptic circuit (grey box) which contributes to the activity signal at the time of presynaptic stimulation: dotted arrow leading from synaptic switches to adaptation circuit in (c). (c) Analog circuits for the adaptation mechanism consisting of three blocks. See text for details. Comparator output drives leakage conductance of dendrite: dashed arrow leading to (b). (d) Current–voltage ( $I$ – $V$ ) relationship of the comparator.

separate transistor T1x. Transistor T2 determines the magnitude of  $I_{in}$  according to its gate voltage SIIN (signal in). The current mirror changes the sign of the current. The  $V_{si}$  dynamics are as follows:

$$\dot{V}_{si} = \frac{1}{C_{si}} (I_{Buf} + I_{in}) \quad (1)$$

where  $I_{Buf}$  is the output current of FI2 whose size is determined by the bias voltage SIBUF [19]. SIREST is a reference voltage representing the signal resting level.

*Step 2:* Low-pass filtering of  $V_{si}$  occurs by the follower integrator FI3

$$\dot{V}_{se} = \frac{I_{SETAU}}{C_{se}} (k(V_{si} - V_{sc})) \quad (2)$$

where  $I_{SETAU}$  is the amplifier's bias current whose size is determined by the bias voltage SETAU, and  $k$  is a constant associated with the amplifier [19].

*Step 3:*  $V_{se}$  is compared against SEREF by a wide-range input differential pair [20]

$$I_{leak} = I_{maxleak} \tanh \frac{\kappa}{2} (V_{se} - SEREF) \quad (3)$$

where  $I_{maxleak}$  is the bias current of the differential pair, representing the maximal leakage conductance, which is determined by the bias voltage GMAXLEAK. The resulting leakage current,  $I_{Leak}$ , is converted by a diode-connected transistor D1, into a voltage  $V_{GLEAK}$ , which is used as the gate voltage of the follower-integrator emulating the  $RC$  circuit of a compartment [13]. This closes the adaptive, negative feedback loop. When  $V_{si}$  is rising due to synaptic activity in the dendrite, the leakage conductance increases, inhibiting in turn the membrane potential. Fig. 1(d) depicts the current voltage relationship of the wide-range input differential pair being a sigmoid [19], [20]. The knee point of the sigmoid is given by the gate voltage SEREF. The limiting factor in the adaptation range is the small linear range of the follower integrator FI2. Its output  $V_{si}$  has to be kept within a range of 100 mV (above SIREST, marked by “operating range of  $V_{si}$ ”). Higher voltages cannot be followed due to the short linear range of the amplifier [19]. To ensure that  $V_{si}$  stays in this small linear range, we adjust the parameter SIIN when all synaptic circuits are stimulated with maximal frequency.

Figs. 2–4 show recordings from a fabricated chip. We have designed a four-compartment neuron, in which three compart-

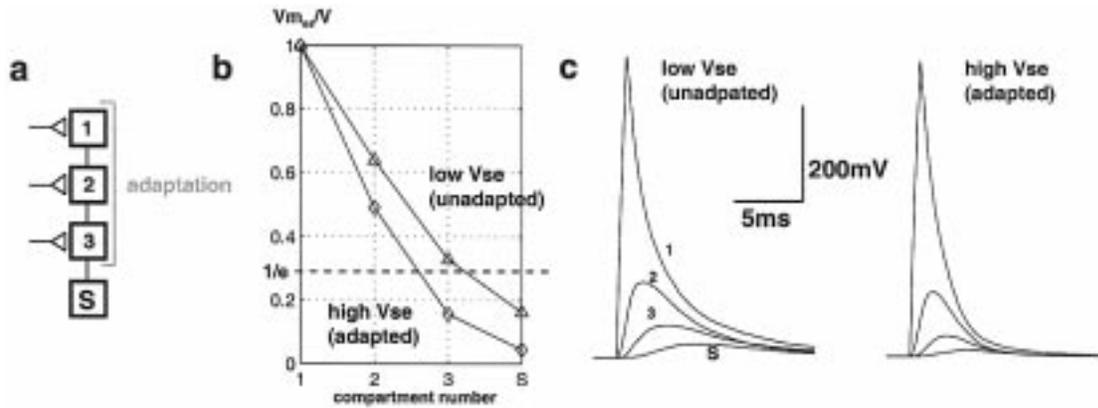


Fig. 2. Spreading properties of the adaptive dendrite. (a) Neuron model: A four-compartment neuron in which three compartments are dendritic compartments (1, 2, 3) and one is the somatic compartment (s). Each dendritic compartment contains a synaptic conductance. Adaptation is based on one activity signal for the three dendritic compartments. (b) Spreading properties for two values of  $V_{se}$ , SIREST = 2.0 and 2.1 V. (c) EPSP propagation for two different values of  $V_{se}$ , SIREST = 2.0 and 2.1 V, SEREF = 2.15 V, GMAXLEAK = 4.38 V.

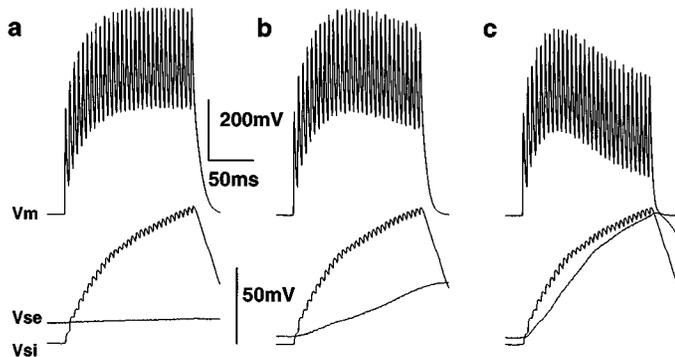


Fig. 3. Response of a single compartment  $V_m$  and the corresponding activity variables ( $V_{si}$ ,  $V_{se}$ ) to presynaptic stimulation. (a) SETAU = 0 V: no adaptation occurs. (b) SETAU = 0.1 V: medium adaptation occurs, the sum of EPSPs decreases about 20 ms after onset of stimulation. (c) SETAU = 0.2 V: high adaptation occurs immediately. SIIN = 0.25 V; SIBUF = 0.21 V. Remaining parameter values as in Fig. 2.

ments are dendritic compartments each containing an excitatory synapse [Fig. 2(a)]. The fourth compartment is the soma and contains the spiking mechanism. The three dendritic compartments are regulated by the same activity signal. A chip was fabricated using standard 1.2- $\mu\text{m}$  CMOS technology. Transistor sizes are generally 6  $\mu\text{m}$  by 6  $\mu\text{m}$ . The following results show recordings from this chip.

### III. RESULTS

We begin the analysis of our adaptating dendrite by determining the desired electrotonic properties. We stimulate a dendritic compartment with a step current to adjust the space constant by tuning the cable parameters. When the voltages have saturated, we measure the steady-state voltage of each compartment and plot it against the dendritic location (the compartment number) [Fig. 2(b)]. This gives us a measure for the electrotonic spread in the dendrite [13]. We do these spread measurements for the minimal and maximal value of the activity signal (and sensor) to simulate the two extremes of adaptation. In the case of a low activity signal (SIREST low), electronic spread reaches

into the fourth compartment, showing a steady-state depolarization of about 180 mV. In the case of a high activity signal (SIREST high), electrotonic spread reaches only significantly into the third compartment. Another way to get an intuition for the two extreme values of propagation is to look at the excitatory-postsynaptic potential (EPSP) spread in the two different conditions [Fig. 2(c)]. An EPSP elicited at one end of the dendrite (compartment 1) spreads toward the somatic compartment while decaying in amplitude and broadening in width [13].

Next, we look at EPSP summation in a single compartment and how adaptation proceeds for three different values of SETAU (Fig. 3). A single synapse was stimulated with a presynaptic train of spikes. The activity signal was tuned to have a decay time constant of about 20 ms in order to keep the activity signal in the linear range of the transconductance. The activity signal increases identically in all three cases because of identical synaptic stimulation. The activity sensor, however, increases in proportion to the value of the parameter SETAU and leads therefore to different EPSP summation. In case of no adaptation, the EPSPs sum up and saturate due to the leakage and axial conductance in the cable [Fig. 3(a)]. For a medium value of SETAU, adaptation becomes evident after about 50 ms [Fig. 3(b)]. For a high value, adaptation occurs very fast [Fig. 3(c)]. This fast form of adaptation should not be confused with synaptic depression, in which the amplitude of the EPSP decreases. Here, it is the increasing leakage conductance that repolarizes the membrane potential and leads to inhibition. In the remaining recordings, we chose slow adaptation dynamics, which is biologically more plausible (see Section IV).

We now turn to I/O relations of the adaptating dendrite. In all these experiments, the input is a presynaptic frequency (F) either to a single synapse or to all of the three synapses in the dendrite. The output is always measured when adaptation has reached its steady-state. The resulting output is either a voltage (V) of a compartment or of the soma, or the somatic spike frequency (F). We term these plots the voltage–frequency curve (V–F curve) and the frequency–frequency curve (F–F curve), respectively.

We expect that the slope of these adapted I/O-relations will be shallower than the slope for the unadapted ones, as shown in Fig. 4(a). To test this I/O relation first on a compartment,

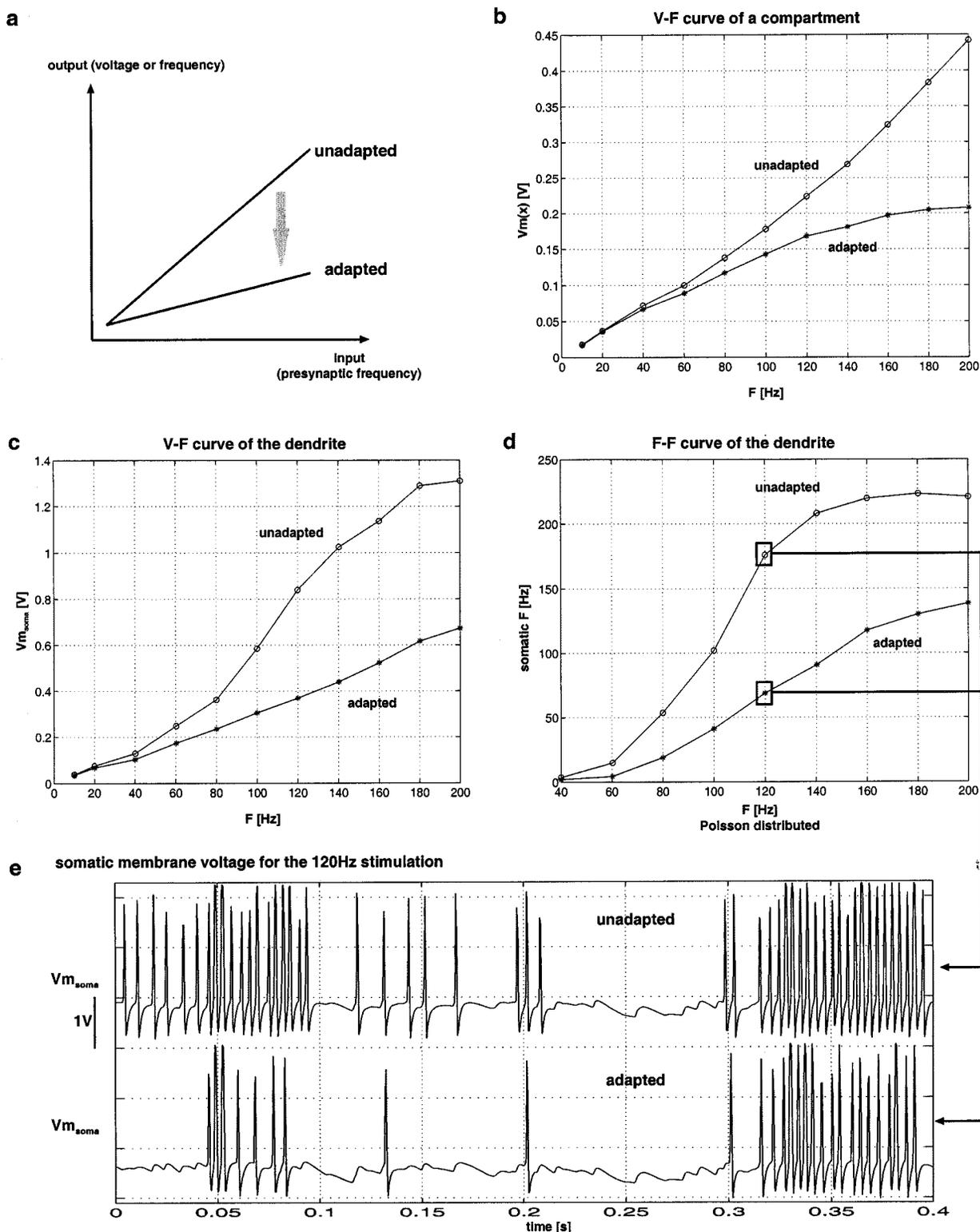


Fig. 4. I/O relations for unadapted and adapted compartments and dendrites. (a) Schematic graph of adaptation. (b) Voltage-frequency curve for a dendritic compartment.  $SIIN = 0.21$  V. (c) Voltage-frequency curve for a branch.  $SIIN = 0.15$  V. (d) Frequency-frequency curve for a branch.  $SIIN = 0.15$  V. (e) Somatic membrane voltage for the 120 Hz stimulation of (d). Neuron parameter values: resting potential = 2.0 V, spiking threshold = 2.6 V, sodium reversal potential = 5.0 V, potassium reversal potential = 1.5 V. Remaining parameter values as in Fig. 2.

we stimulate the synapse of one compartment and measure the average membrane potential when adaptation has reached its steady-state. The resulting voltage-frequency curve is shown in

Fig. 4(b). The V-F curve for the unadapted case is steadily increasing, while the adapted V-F curve saturates due to the increasing leakage conductance. We obtain a similar curve for the

V–F curve of the dendrite [Fig. 4(c)], where the three synapses were stimulated with the same frequency and the membrane voltage in the soma was measured. The adapted curve does not saturate because the somatic leakage conductance is not regulated in our model. Finally, we measure the F–F curve of the dendrite with more realistic input conditions [Fig. 4(d)]. We use Poisson distributed spike trains as inputs to the three synapses. In the soma we measure the output frequency of the spiking mechanism. The almost sigmoidal F–F curves for both the unadapted and adapted case are partly due to the nonlinear behavior of the spiking mechanism [17]. Fig. 4(e) shows the somatic membrane voltage for one presynaptic stimulation frequency. The synaptic stimulation pattern is exactly the same for both the unadapted and adapted case, which is best evident if one compares the subthreshold membrane fluctuations between the times 0.22 and 0.3 s.

#### IV. DISCUSSION

Various forms of plasticity have already been implemented in aVLSI neurons with the purpose of exploring these adaptive effects in an analog electronic neural networks. At the *somatic* level, both the short- and long-term forms of adaptation, spike frequency adaptation and regulation respectively, have been implemented [21], [22], [17]. Both forms are based on a model of intracellular calcium concentration in the soma. In the case of spike frequency adaptation, the calcium sensitive channel is the after-hyperpolarizing conductance, which inhibits the membrane voltage [21], [17]. In the case of regulation, the leakage conductance is modified by activity sensors reporting the variance and mean level of calcium [22]. In these two forms of adaptation, the neuron regulates its own (spiking) output. At the *synaptic* level, short-term depression was implemented [18]. Synaptic depression is the phenomenon of a decreasing EPSP amplitude in response to an increasing input frequency. A single synapse acts in this way adapting to its own input. We have now presented adaptation in a dendrite which can be seen as an intermediate form between somatic and synaptic adaptation. In contrast to synaptic depression, dendritic adaptation is un-specific to the input because it responds to the pool of synaptic input. However, it is specific to the neuron's output, because a reduced depolarization in the dendrite leads to a reduced output frequency. This form of dendritic adaptation could therefore be seen as a part of a continuum of forms of adaptation from the input side (the synapse) to the output side (the soma).

We have not yet specified the activity signal. In our work, the dynamics of the activity signal are too fast (time constant 20 ms) to represent any known signal. To yield slower dynamics, for example, comparable to intracellular calcium concentration (decay time constant of about 100 ms [1]), the capacity and linear range of FI2 had to be increased. The activity signal was then low-pass filtered at a slow rate to model adaptation on a long time scale. This seems reasonable given the increasing number of computational models that support a model of calcium-mediated long-term adaptation via various calcium sensors [23], [3], [4]. To yield very slow dynamics however, on the order of 500 ms and more, a different delay scheme, for example using floating gates, had to be implemented.

Another way to exploit such an adapting mechanism is to simulate the concentration of a neuromodulator. Neuromodulators can change the integration properties of neurons substantially [24], [25]. One modeling study even exploits this mechanism to explain binding and segmentation of visual scenes [11]. In that model the leakage conductance of the dendrite was changed to achieve an altered synaptic integration in a similar way as in our circuits.

The design of the circuits is modular. Adaptation could easily be constructed for more elaborate dendrites having several branches with independent adaptation. Thus, the adaptive dendritic circuits presented here can well be the basis for building highly dynamic networks as different engineering groups pursue it [26], [27], [21].

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