

Forward- and Backpropagation in a Silicon Dendrite

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Abstract—We have developed an analog very-large-scale integrated (aVLSI) electronic circuit that emulates a compartmental model of a neuronal dendrite. The horizontal conductances of the compartmental model are implemented as a switched capacitor network. The transmembrane conductances are implemented as transconductance amplifiers. The electrotonic properties of our silicon cable are qualitatively similar to those of the ideal passive cable that is commonly used to model mathematically the electrotonic behavior of neurons. In particular the propagation of excitatory postsynaptic potentials is realistic, and we are easily able to emulate such classical synaptic integration models as direction selectivity. We are also able to emulate the backpropagation into the dendrite of single somatic spikes and bursts of spikes. Thus, this silicon dendrite is suitable for incorporation in detailed silicon neurons operating in real-time; in particular for the emulation of forward- and backpropagating electrical activities found in real neurons.

Index Terms—Analog very-large-scale integrated (aVLSI), backpropagation, dendrite, neuromorphic engineering.

I. INTRODUCTION

THE DENDRITES of neurons have a rich repertoire of electrical properties that support signal processing [1]. Because experimental studies can demonstrate so different and sometimes contradicting signal processing, computational models of dendrites are diverse as well. We classify the models into four groups that are convenient for the discussion of dendritic processing. These groups are: passive, active, adaptive, and models accounting for backpropagation¹ of spikes.

Traditional computational models for dendritic processing model the dendrite as a *passive*, branched cable structure. This view was originated by Rall in the 1960s (see [2] for a review) and is still popular [1], [3]. However, in recent years it has become clear that dendrites have many, highly nonlinear properties that arise from the many voltage-dependent *active* conductances that are found in the membranes of the dendritic tree [1], [4]. Computational models that account for these nonlinearities are as diverse in their functionality as the experimental findings [5]–[7]. Common to all these passive and active computational approaches is the idea that synaptic input is somehow combined and conveyed—or what we now term “forward-propagated”—toward the soma in an essentially analog process. Recently, another crucial feature of dendritic processing has been attracting attention: the *backpropagation* of somatic spike

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¹In this context, backpropagation means propagation of somatic spike activity back into the dendrite. Many neural-network modelers interpret this phenomenon as an evidence for a possible mechanism of the backpropagation learning used in artificial multilayer networks.

events into the more distal dendrites [8]. Backpropagation is an active process, but of course, passive electronic spread of the spike signal into the dendrite also occurs [9]. Theoreticians, who study the computations performed by neurons, are now incorporating backpropagation in their neuronal and network simulations and electronic emulations [10]–[13]. Finally, there is evidence for *adaptive* dendritic properties. Ionic conductances in the dendrite can change in response to cellular biochemical signals; and these conductance changes consequently cause changes in electrotonic spread [14]–[16]. Although adaptive processes have so far been less popular with theoreticians, they are now also being recruited to models of dendritic computation [5], [17]. However, the relative importance of these dendritic modes of signal processing in the various dendrite models is still unclear.

What is clear, is that the study of highly distributed active processes is computationally expensive when simulated on conventional computers. On the other hand, analog very-large-scale integrated (aVLSI) circuits offer the possibility of emulating these processes physically, in real time. Such emulations open the route for high-speed qualitative modeling investigations, and for the possible construction of hardware neuronal networks that can perform useful signal processing [18]. We have previously described our methods and results in the construction of active and passive conductances suitable for the fabrication of simple silicon neurons, which emphasized the electrophysiology of the somata [19], [20]. More recently, we have focused on developing neuromorphic dendrites and synapses [21]–[23] that could be used as the basis for exploring the above mentioned modes of dendritic computation. Elias’ group has already successfully built silicon dendrites with integrate-and-fire somas [24] that account well for the passive mode of dendritic operation. In contrast, we report here a passive dendrite with good performance, that incorporates also voltage-dependent ionic conductances of the kind observed in the somata and dendrites of real neurons. Our silicon dendrite can therefore be used to explore both passive and active synaptic forward- and backpropagation phenomena.

II. METHODS

The common approach to modeling dendrites is to transform the dendrite into an approximation to a cable [25]. The dendrite is discretized into connected segments of dendritic cylinder, so-called compartments [Fig. 1(a)]. A minimal compartment comprises an *RC* circuit representing the electrical passive behavior of that cylinder of membrane; and axial resistors representing the axial resistance (or internal resistance) between the centers of the successive dendritic cylinders. The translation of these simple circuits into aVLSI circuits, meet an immediate problem: the implementation of resistors. The aVLSI

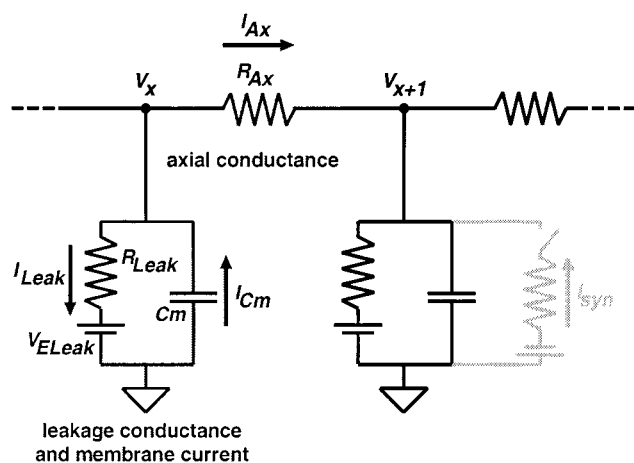
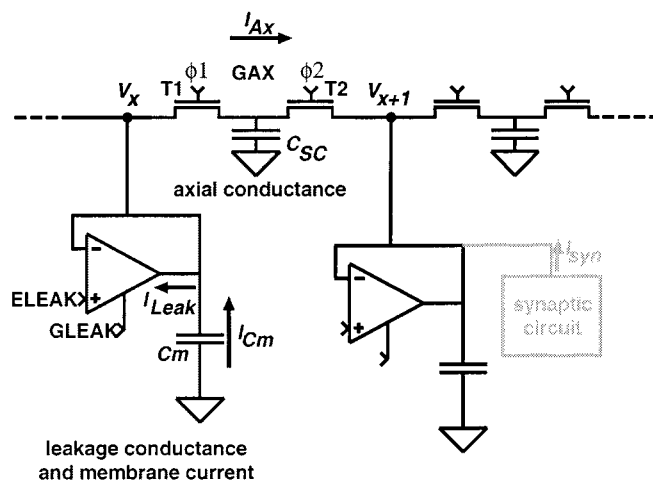
a compartmental model

b implementation


Fig. 1. Compartmental modeling in theory and silicon. (a) Electrical diagram of a compartmental model of a piece of dendrite: RC circuits (leakage conductance and membrane current) are connected by axial conductances. The capacitance C_m represents the membrane capacitance across which the membrane current, I_{Cm} flows. The resistor R_{Leak} simulates the membrane resistance, through which current (I_{Leak}) leaks away. The battery V_{ELeak} represents the resting potential of the entire neuron. The node, V_x (V_{x+1}), represents the membrane potential in compartment x ($x+1$). R_{Ax} simulates the axial resistance, through which the axial current, I_{Ax} flows. In the right RC element, a synaptic circuit is shown in gray. (b) Silicon implementation of (a). The RC circuit is approximated by a follower circuit, the axial resistor by the switched capacitor method ($\phi 1$ and $\phi 2$ are the two nonoverlapping clocks feeding transistor T1 and T2, respectively). The gray “synaptic circuit” schemes indicate where a current from a synaptic aVLSI circuit is dumped onto. In our circuits we use (neurophysiological) conductance notation: G_{LEAK} corresponds to $1/R_{Leak}$, G_{AX} to $1/R_{Ax}$ (later given as frequency). $E_{LEAK} = V_{ELeak}$.

technology lends itself to the fabrication of active elements (transistors), capacitors, and connecting wire; but not to the simple construction of fixed resistors. Various approximations to resistors and RC circuits are possible in aVLSI circuits; each with advantages and disadvantages [26].

In our silicon dendrite, we approximate the membrane RC circuit by a follower integrator [Fig. 1(b)], which we have already successfully used in our silicon neuron [20]. The dependence of the leakage current I_{Leak} on the membrane voltage V_m is given by the current–voltage relationship of the transconductance amplifier of the following:

$$I_{Leak}(V_m) = I_{GLEAK} \tanh\left(\frac{\kappa}{2U_T}(E_{LEAK} - V_m)\right) \quad (1)$$

where

- I_{GLEAK} bias current of the amplifier, whose magnitude is determined by the voltage G_{LEAK} ;
- κ gate efficiency constant ($\kappa \simeq 0.7$);
- U_T thermal voltage ($U_T \simeq 0.025$ V at room temperature).

The amplifier is linear over a differential input voltage range of about 100mV. In this (small) linear region, the follower integrator acts as an ideal RC circuit, outside the linear region, the amplifier provides a fixed current. We emulate the axial resistance by the switched-capacitor method, which was applied by Elias *et al.* for their artificial dendritic trees [24], [27], [28]: Two nonoverlapping clocks ($\phi 1$, $\phi 2$) drive two transistors (T1, T2). The actual conductance value of the resistor is given by multiplying the clock frequency by the capacitance (C_{SC}). We call it G_{AX} in accordance to our general neurophysiological notation of conductances [19] and give values of G_{AX} in Hertz as this is the value we set to this conductance.

We chose the transconductance amplifier as RC circuit, because it gives us the opportunity to further extend the dendrite with self-adapting circuits. That this is possible has already been shown on the silicon neuron [29] (see also discussion “adaptive”). As horizontal resistor we preferred the efficient switched-capacitor method over other approaches (e.g., HRES by Mead [26]) to compensate for the small linear region of the transconductance amplifier. Because the clocks consume a lot of power, the circuit loses the neuromorphic appeal of low-power. Yet, we need to set only one value of G_{AX} because the axial resistance of a dendritic cable is supposed to be the same for different neuron types. To avoid capacitive coupling of the clock signals with the analog voltages, we have designed our layout as in Elias work [28].

We have constructed various dendrite models. To test the effect of cable termination (also called boundary condition) on passive electrotonic spread we have implemented dendrites of different length (four to ten compartments). To test synaptic propagation and integration, four- and five-compartment models were developed, in which compartments include also synaptic conductances. The construction and performance of the synaptic conductances has been described previously [22]. We stimulate our synaptic circuits with pulses of 1ms width, which represent action potentials. The synaptic current of the synapse has the following approximate dynamics: During the first ms, the current increases, then it decays as $1/\text{time}$ with a duration of about 1 to 2 ms. The pulse trains are generated by a general purpose electronic interface card (National Instrument LabPC+) controlled by a computer.

We explored the active propagating properties of the dendrites using a set of ionic conductances developed for a silicon pyramidal cell [20]. These conductances include the typical spiking conductances (sodium and potassium conductance), a model of

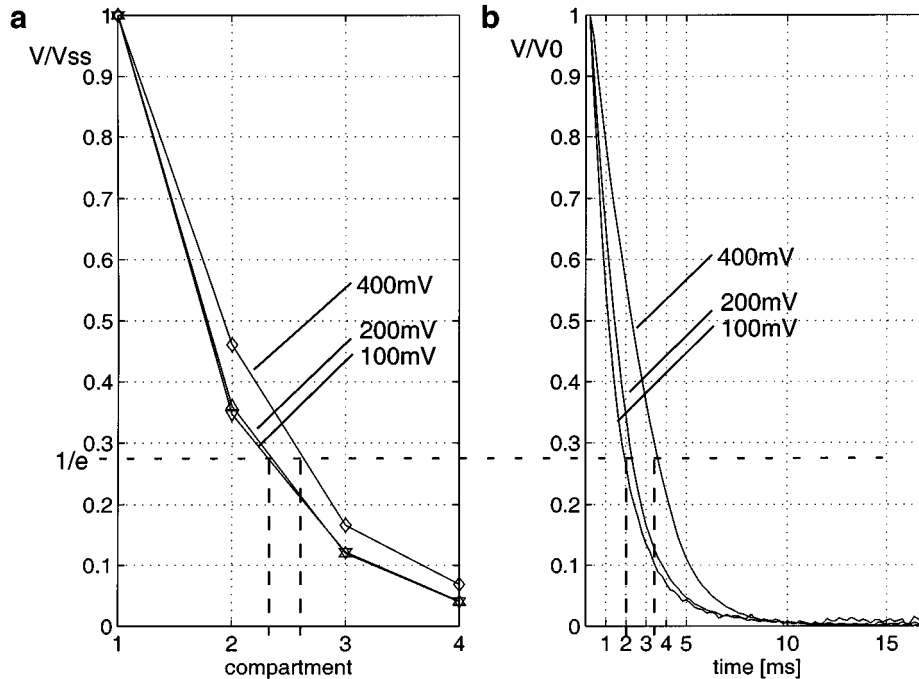


Fig. 2. Space and time constants in the silicon cable. (a) Voltage gradient along the compartments for different steady-state voltages ($V_{ss} = 100$ mV, 200 mV, 400 mV). Dashed vertical lines: space constants. (b) Decay of V_m from different initial voltages ($V_0 = 100$ mV, 200 mV, 400 mV). Dashed vertical lines: time constants. Parameter values: $G_{LEAK} = 0.26$ V, $G_{AX} = 10$ kHz, $E_{LEAK} = 2.0$ V.

the somatic intracellular calcium concentration and a calcium dependent after-hyperpolarizing conductance. With these ionic conductances an aVLSI soma is able to fire in three different spiking modes: fast spiking, regular spiking, and bursting. Fast spiking requires only the sodium and potassium conductances for generating spikes. Regular spiking is spiking with spike frequency adaptation (with increasing interspike intervals) based on a model of the intracellular calcium concentration and the after-hyperpolarizing conductance forming a negative feedback loop [20]. Bursting is high-frequency spiking with long periods of silence between bursts and is based on the same ionic conductances as for regular spiking but operating under slightly different dynamics. These ionic conductances are placed in one end of a compartmental dendrite, representing the somatic compartment.

Our results are drawn from a number of test chips (2.2 mm)², that were fabricated using standard 1.2 μ m CMOS technology. Our circuitry uses only a small fraction of this area. Transistor sizes are generally 6 μ m by 6 μ m. The membrane capacitance C_m per compartment is about 1 nF. For reasons of testing, we used two significantly different sizes of C_{SC} . In one type of cable, C_{SC} is only the parasitic capacitance (< 1 pF) between the two switching transistors. In the other type of cable, C_{SC} consists of a poly-poly2 capacitor of the size of approximately 10 pF. Because of these two significantly different sizes of C_{SC} , we also have two significantly different ranges of G_{AX} values. The transconductance amplifier is designed as in Mead's circuits [26], the switched capacitors are designed as in Elias' layouts [28].

III. RESULTS

As a first step in our analysis we adjust and determine the space and time constant of our silicon cable (also called length

and membrane time constant, respectively) by using a simple exponential measure. While in computer simulations the parameter values of the cable (axial and leakage conductance, membrane capacitance and diameter) are given directly by experimental and anatomical studies, we cannot directly translate such experimental values into the parameter voltages of the silicon dendrite. Instead, the parameter voltages must be adjusted to yield the same electrotonic qualities observed in the real dendrites. The decay of voltage from different steady-state voltages (elicited by a step current in one end of the cable) is shown in Fig. 2. Because our silicon cable model does not contain any information about the morphology (geometry) of a neuron, we can not calculate a space constant in absolute distance. We therefore measure the space constant in units of compartments by determining the dendritic location after the voltage has decayed to 37% ($1/e$) [Fig. 2(a), dashed lines]. The measured space constants range between one and two compartments. We determine the time constant by a similar method to the space constant: we measured the time taken for the voltage to decay to 37% of its initial value [Fig. 2(b), dashed line]. The range of the time constants is about 2 ms to 3.5 ms. The differences are due to the small linear region of the amplifier that represents the membrane RC circuit. For large amplitudes the amplifier merely provides a constant current, which causes the slower decrease of the membrane voltage at high depolarizations. Therefore, both space and time constant are greater for high amplitudes (large depolarizations) than for small amplitudes (small depolarizations).

In a next step, we examined the effect of the cable parameter values, such as axial conductance, the leakage conductance and the length of the dendritic cable, on electronic spread (Fig. 3). A high value for the axial conductance G_{AX} causes the electrical signal to propagate further, yielding a larger space con-

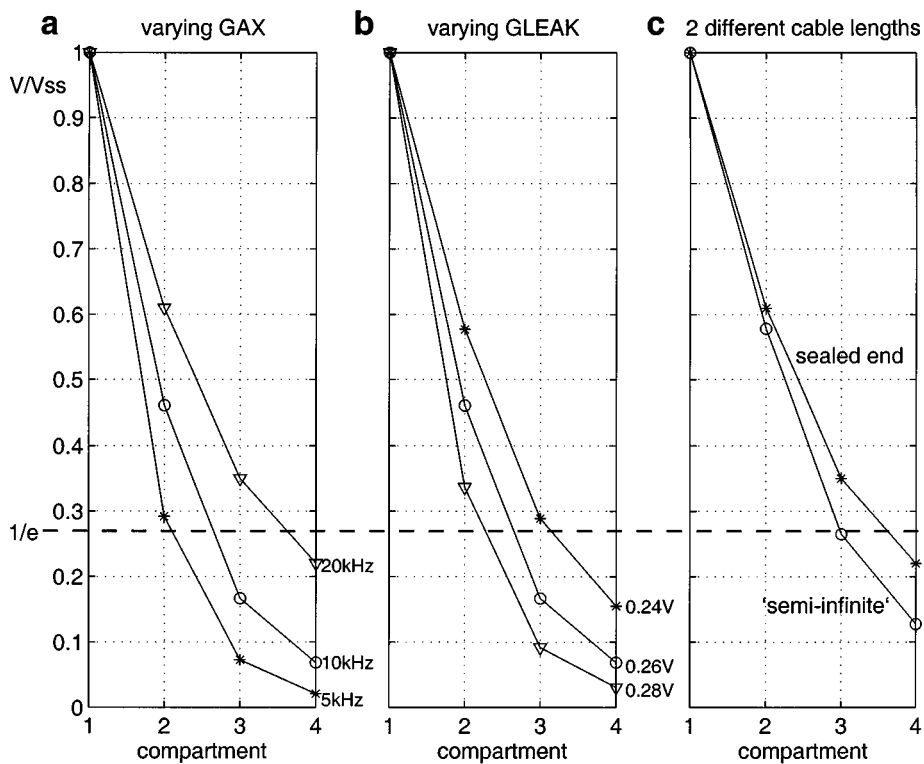


Fig. 3. Electrotonic spread for different cable parameters and cable lengths. (a) Spread for different values of GAX (20 kHz, 10 kHz, 5 kHz). $GLEAK = 0.26$ V. (b) Spread for different values of $GLEAK$ (0.24 V, 0.26 V, 0.28 V). $GAX = 10$ kHz. (c) Comparing spread in a four- and a ten-compartment model, sealed end and “semi-infinite,” respectively. $GLEAK = 0.26$ V, $GAX = 20$ kHz. (a)–(c) $V_{ss} = 400$ mV.

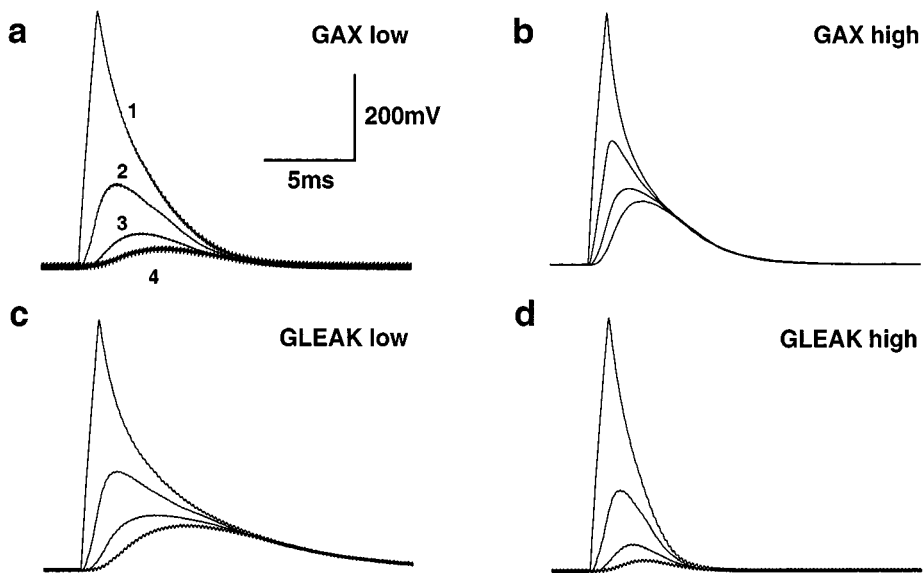


Fig. 4. Spread of an excitatory postsynaptic potential (EPSP) along the cable for different conductance values. A synaptic conductance at one end of the cable is stimulated. The amplitude of the resulting EPSP is adjusted to about 600 mV. The membrane potentials of the stimulated compartment (1) and the following compartments (2, 3, 4) are shown. $E_{LEAK} = 2.0$ V. In (a) and (b), $GLEAK (= 0.25$ V) is fixed and GAX is varied: (a) $GAX = 15$ kHz. (b) $GAX = 50$ kHz. In (c) and (d), $GAX (= 20$ kHz) is fixed and $GLEAK$ is varied: (c) $GLEAK = 0.22$ V. (d) $GLEAK = 0.28$ V. The “noise” on some of the membrane voltages derives from the low clock frequencies for GAX .

stant than for a lower value of GAX [Fig. 3(a)]. A high value for the leakage conductance $GLEAK$ causes to leak the electrical signal away faster and so to propagate shorter, yielding a smaller space constant than for a lower value of $GLEAK$ [Fig. 3(b)]. Fig. 3(c) compares the electrotonic spread in two different cable lengths, a four- and a ten-compartment model.

The space constant for the short cable is larger than for the long cable. The spread in the four-compartment model is analogous to the sealed end termination, or simply a short cable in which the charge accumulates at one end. The ten-compartment model is an approximation to a semi-infinite cable, a cable of infinite length in one direction. In this case, charge in the fourth com-

partment is more attenuated in comparison with the four-compartment model, because the charge is propagated further down the cable, which thus results in a smaller space constant. These measurements agree qualitatively well with the calculations of cable theory (see [30] for a comparison).

The previous two figures illustrated the response of the cable to artificial current signals (step currents) used to explore basic properties of the silicon cable. We turn now to a more realistic input, the synaptic input. Fig. 4 shows the propagation of an excitatory postsynaptic potential (EPSP) along the dendrite for different axial and leakage conductances of the dendrite. In each experiment, the amplitude of the EPSP is adjusted to the same value for comparison. Fig. 4(a) and (b) show the time course of EPSP propagation for two extreme values of G_{AX} . For a low G_{AX} , the space constant is small and hardly any depolarization occurs in the third and fourth compartment. For a high G_{AX} the space constant is large and depolarizations in the third and fourth compartment are still noticeable. In Fig. 4(c) and (d), we varied the value of G_{LEAK} . For a low G_{LEAK} , the time constant is large and the EPSP propagation looks similar to the one in Fig. 4(b). For a high G_{LEAK} , the time constant is decreased. The duration of the EPSPs is between approximately 6 ms and 13 ms [Fig. 4(c) and (d), respectively]. The shape, duration, and spread of our silicon EPSPs (Fig. 4) compare favorably with real EPSP's (see, for example, [31, p. 416] and [32, p. 99]).

Next, we investigated the passive propagation of somatic spike signal into the dendrite. We test a four-compartment model, in which one compartment contains the ionic conductances of a pyramidal soma (Fig. 5). We stimulated the somatic compartment with a step current in each of the three different spiking modes. A spike elicited in the soma propagates passively backward into the dendritic compartments while decaying in amplitude and broadening in width due to the low-pass filter properties of the dendritic cable: Spikes in the soma are of 1 ms duration and of full amplitude, in the distal compartment of 3ms duration and almost flattened in amplitude [Fig. 5(a) and (b)]. The effect of a burst is much more significant [Fig. 5(c)]. A burst in the soma can be seen as a very wide spike invading the dendritic compartments.

Now we test the ability of the silicon dendrite to realize a simple model of dendritic function. The retina, thalamus and visual cortices contain neurons whose response is sensitive to the direction of motion of a visual stimulus across their receptive field [33]. The biophysical mechanism causing this direction selectivity is not yet fully explained. However, there are a number of models that try to explain this mechanism by synaptic interactions within dendrites [1, p. 130]. One popular model, originally suggested by Rall [34], is that direction selectivity is due to the asymmetrical summation of EPSPs that occurs in dendrites when synapses distributed along the dendrite are activated sequentially, either toward, or away from the soma (see [35] and [36] for a recent contribution to that debate). Fig. 6 shows the ability of a five-compartment model to achieve this kind of direction selectivity. The somatic compartment contains the spiking mechanism, each of the four dendritic compartments contains a simple excitatory synapse. The synaptic conductances are stimulated sequentially, first from the distal end of the dendrite toward the soma (the preferred direction), and

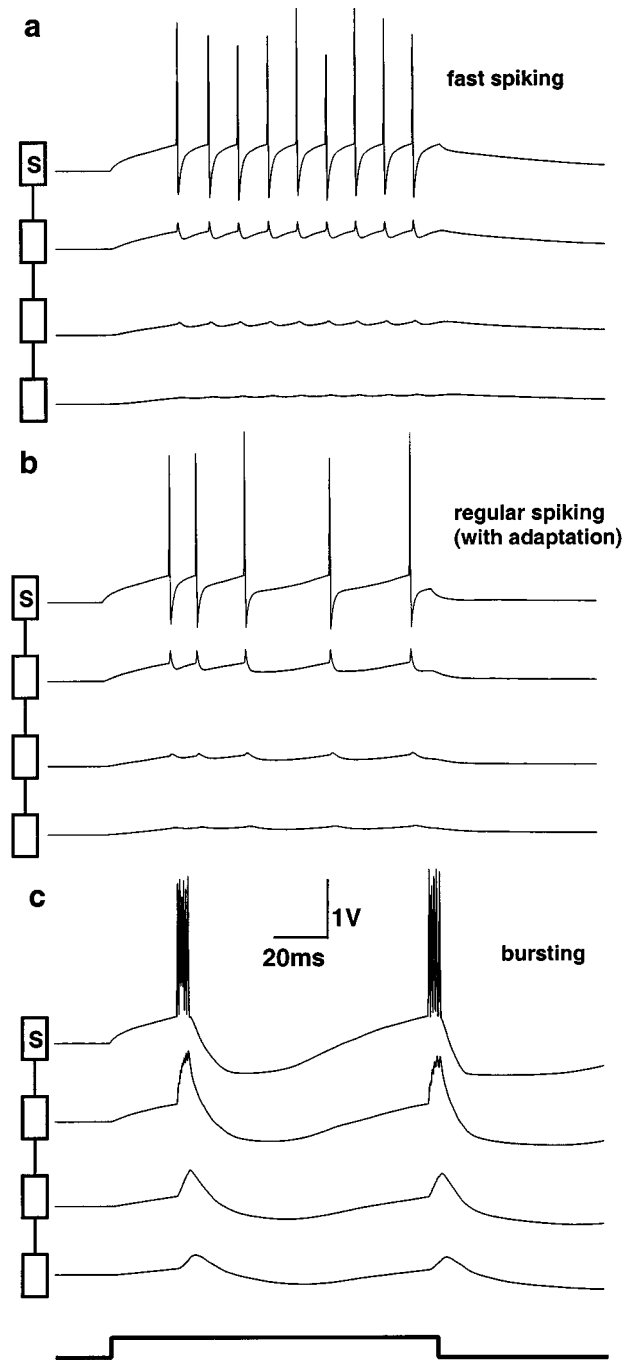


Fig. 5. Influence of somatic spikes on the silicon dendrite. The same step current [120 ms, indicated below (c)] has been applied to the somatic compartment ("S") of the silicon dendrite (see iconized form on the left) for different somatic spiking modes. (a) Fast spiking. (b) Regular spiking (with adaptation). (c) Bursting. Parameter values: $G_{LEAK} = 0.22$ V, $G_{AX} = 200$ kHz, $E_{LEAK} = 2.0$ V. Relevant soma parameter values: sodium reversal potential = 5.0 V, spiking threshold = 2.5 V, potassium reversal potential = 1.5 V.

then from the soma toward the distal end (the null direction). In the preferred direction, the EPSPs sum up toward the soma and yield a large depolarization that exceeds the spiking threshold [Fig. 6(a)]. Stimulation in the null direction causes the EPSPs to sum up into the distal part of the dendrite, where the large depolarization has no effect on the spike output of the neuron [Fig. 6(b)].

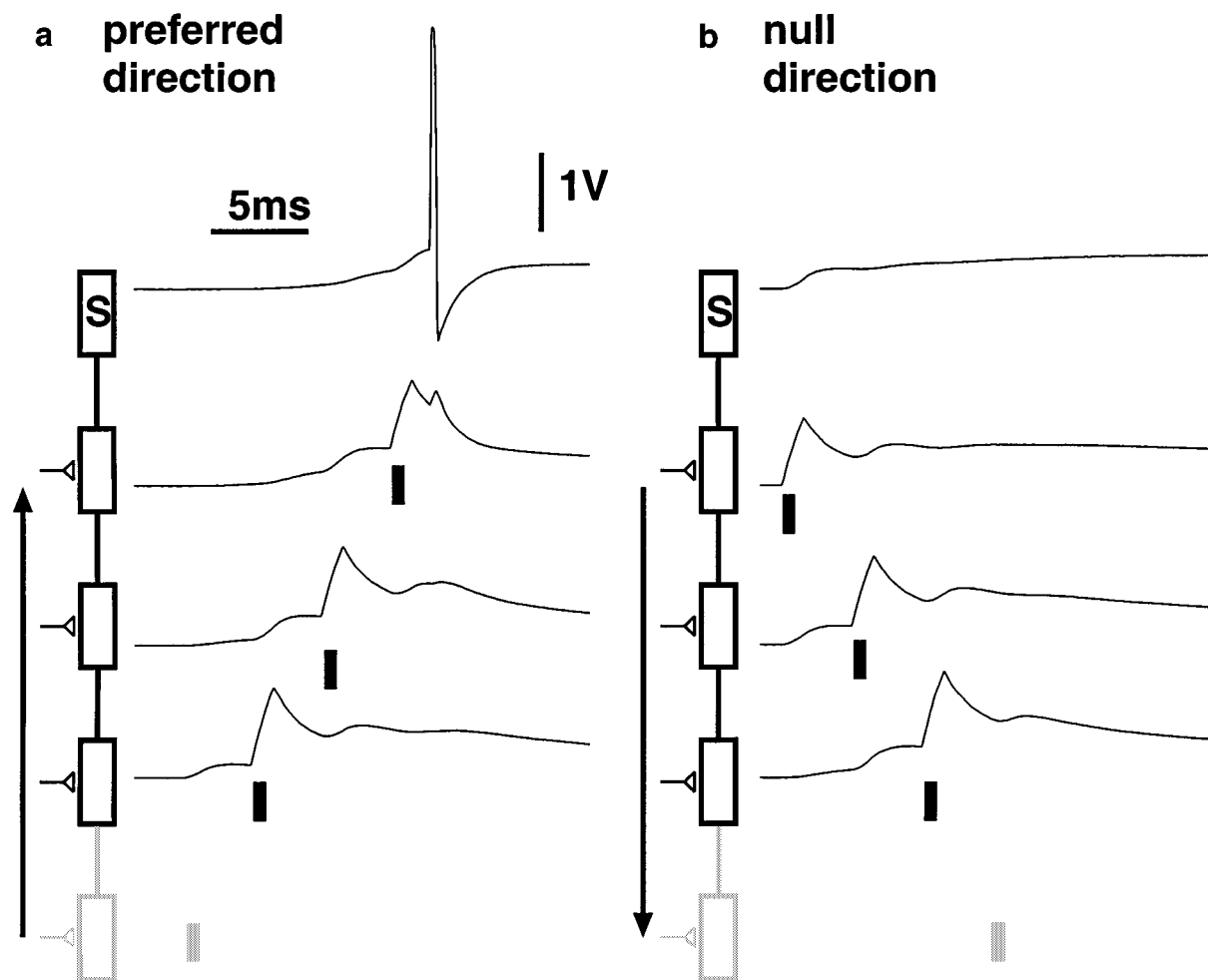


Fig. 6. Direction selectivity of the silicon dendrite. (a) Each synapse (one per compartment) is stimulated once (vertical black bars), beginning from the distal compartment (membrane potential not shown). The EPSPs sum up in the preferred direction toward the soma and elicit a spike there. (b) Stimulation in the null direction does not elicit a spike because the EPSPs sum up toward the distal compartment of the dendritic cable. Parameter values: as in Fig. 5. EPSP amplitude: ca. 1 V. Presynaptic interspike intervals: 3 ms.

IV. DISCUSSION

We see the circuits as a basis for constructing more elaborate dendrites of the four classes of dendrite models mentioned in the introduction. We discuss this in the following sections.

A. Passive

In Figs. 2 and 3 we have tested the passive cable properties. The cable parameters can be easily adjusted to provide time constants that are in the same order—a couple of ms—as the ones of real dendrites. The absolute space constant of the silicon dendrite cannot be directly compared with a space constant of real dendrites because there is no real geometry (length and diameter) in our electronic circuit. We determined the space and time constant by a simple exponential measure, which is not entirely appropriate for two reasons. First, neither the decay in space nor the decay in time is exponential in a dendritic cable of finite length. Second, our silicon dendrite is nonlinear because of the limited linear region of the amplifier. Nevertheless, we chose the commonly used exponential measure to approximate

the time and space constants and the passive behavior of our silicon cable. The decay of V_m , in space and time, is slower for large amplitudes than for small amplitudes (Fig. 2) due to the nonlinear leakage conductance. When the analog electronic circuits were operated in the very small linear voltage region of the amplifier (<100 mV) we could obtain better approximations to the real leakage conductance. However, in this small linear region device mismatch and crosstalk from the clocks can become a problem. Despite the deviation from an ideal cable behavior due to the nonlinear leakage conductance, the behavior of the silicon dendritic is in good qualitative agreement with general cable properties (Fig. 3). EPSPs in Fig. 4 are comparable to EPSPs in Elias' work (e.g., [28, Fig. 1a]). Direction selectivity in silicon dendrites was already shown in Elias dendrites (summarized in [24]). Our goal was to tune the membrane voltage dynamics to more realistic values.

Furthermore, we think that a reduced compartmental model of a pyramidal neuron, e.g., with only five to six compartments as modeled by Bush *et al.* in computer simulations [37], [38], can be realized in our analog electronic circuits. Such a model had to be developed with comparative simulations in one of the

neuron simulation packages, as for example NEURON [39] or GENESIS [40].

B. Active

In contrast to the above discussed passive mode of dendritic operation, active means that there are also voltage-dependent conductances in the dendritic tree that could cause highly non-linear integration. For example, dendritic spikes seems to exist and it has even been hypothesized that action potentials are initiated there [41], [42]. Another example, is the voltage-dependent synaptic conductance NMDA that could give rise to multiplicative interactions between synaptic inputs [43], [44]. We have not demonstrated any such active dendritic processing in this paper. However, because our circuits are modularly designed, it is easy to rearrange circuits to model active forms of dendritic processing. The successful operation of voltage-dependent conductances is shown by the implementation of the somatic conductances operating (Fig. 5). Another possibility would be to pursue Mel's work on NMDA interactions by the silicon voltage-dependent synaptic conductance [22]. A preliminary model has been worked out by Rasche [21].

C. Backpropagating

In most neural network simulations the backpropagating wave of somatic activity is often ignored. However, recent experimental studies on pyramidal cells reemphasize the crucial role for this kind of backpropagation [45]. Fig. 5 shows clearly the profound influence of a somatic spike on the silicon dendritic cable. Although it is a passive backpropagation, the depolarization is still significant in the dendritic compartments, in particular in the case of bursting. Such a depolarization could be the necessary voltage level to amplify the effect of a voltage-dependent ionic conductance as they occur in real dendrites. Such a coincidence of the backpropagating somatic wave and dendritic input to voltage-dependent synaptic conductances has already been exploited in computational models [12].

D. Adaptive

We already mentioned in the method section that we use a transconductance amplifier for the leakage conductance to possibly extend the dendrite with self-adapting circuits. The bias voltage can be easily modified on-chip according to an adaptive mechanism as various other implemented neuronal adaptation circuits have shown [21], [29]. The adaptation of the leakage conductance has consequences for the electrotonic spread [Fig. 4(c) and (d)] and so on the synaptic integration. We have already implemented a model of such an adapting dendrite, but full results from which will be presented on a future work [46].

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