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Silicon Synaptic Conductances

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Abstract. We have developed compact analog integrated circuits that simulate two synaptic excitatory conductances. A four-transistor circuit captures the dynamics of an excitatory postsynaptic current caused by a real AMPA conductance. A six-transistor circuit simulates the effects of a real voltage-dependent NMDA conductance. The postsynaptic current dynamics are modeled by a current mirror integrator with adjustable gain. The voltage dependence of the silicon NMDA conductance is realized by a differential pair. We show the operation of these silicon synaptic conductances and their integration with the silicon neuron (Mahowald and Douglas, 1991).

Keywords: synaptic conductances, AMPA, NMDA, aVLSI, neuromorphic system

1. Introduction

Neuromorphic systems are artificial systems that capture aspects of neuronal function and organization (Douglas et al., 1995; Mead, 1989). They are often realized in analog very-large-scale integrated (aVLSI) circuits. These electrical circuits compute using analog voltages and currents. Such silicon implementations range from vision chips (for example, Mahowald and Mead, 1991) to synaptic implementations such as the ones presented in this article. This method of building neuromorphic systems has become popular in recent years and is called *neuromorphic engineering* (Watson, 1997). By building and operating these systems we hope to gain further insight into computational principles of neural networks and systems.

Silicon implementations of synapses primarily deal with the on-chip weight storage and the learning rule (Diorio et al., 1995; Elias et al., 1997; Häfliger and Mahowald, 1997; Schultz and Jabri, 1995; Westerman et al., 1997). In those silicon synapses, the postsynaptic current is modeled as a simple pulse. Here we present analog circuitry that approximates the dynamics of the EPSC (excitatory postsynaptic current) caused by a typical AMPA and NMDA conductance. The construction of these silicon synaptic conductances was motivated by computational studies and hypothesis about pyramidal cells. The postsynaptic current might play a crucial role, in particular the NMDA conductance. For example, the voltage-dependent NMDA conductance can act in a multiplicative manner (Mel, 1992b) or in a coincidence manner (König et al., 1996).

One of the most pressing contraints in a VLSI design is the limited silicon area. Often, one has a regular array of, for example, photoreceptors or of synapses. A larger number of photoreceptors in a fixed area leads to an image with better resolution, a larger number of synapses leads to a more detailed neuronal model. The synaptic conductances shown here are compact enough to be built in large numbers.

Another important constraint is the number of parameters on the chip. A large number of parameters leads to a huge parameter space and complex wiring in chip designs. The correct parameter space must be found by tuning the parameter values and complex wiring limits the optimal use of silicon area. Therefore, one aims for few parameters. Our synaptic conductances need only a few parameters.

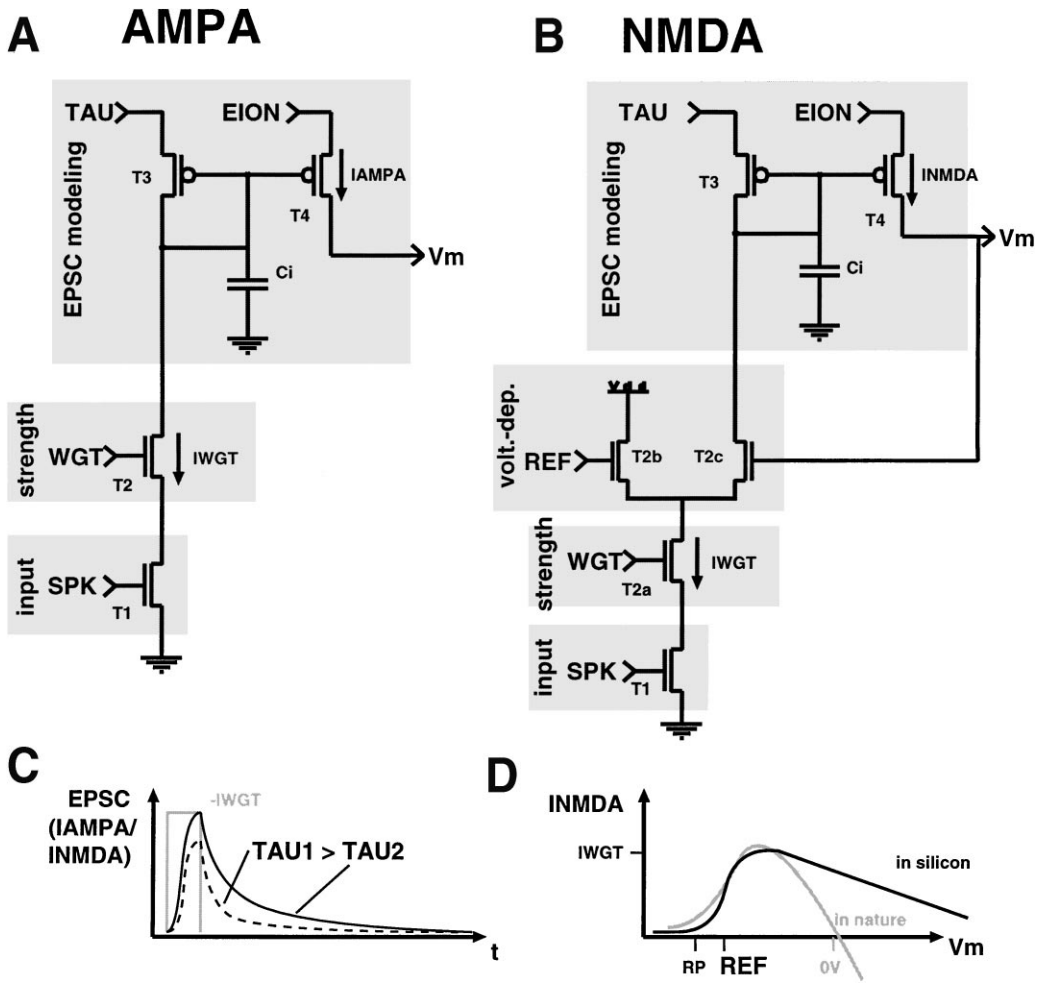

Figure 1. A: Analog circuitry to simulate an AMPA conductance. It consists of an input transistor T1, a weight transistor T2, and a current mirror integrator (T3, T4, Ci) that approximates the EPSC. B: Circuitry of the NMDA conductance. In addition to the AMPA circuit, it contains two differential transistors emulating the voltage dependence. For further details, see text. C: Schematic drawing (not simulation) of the response of the current mirror integrator with adjustable gain to a current input pulse (-IWGT). Two different curves are drawn qualitatively for two values of TAU (solid and dashed lines). D: Qualitative comparison between the current-voltage relation of the silicon and natural NMDA conductance. In nature, the relationship gives rise to a bell-shaped curve (Johnston and Wu, 1995). In silicon, the curve consists of two distinct parts: the upward part is a sigmoid due to the differential pair; the downward part is a linear decay due to the difference between EION and V_{m} on transistor T4. The kneepoint of the sigmoid is set by the voltage REF, the amplitude by the parameter WGT. RP: resting potential.

We show the following measurements from our first chip: the integration of the membrane potential in response to successive stimulation of the silicon AMPA and NMDA conductance and the operation of the silicon synapses in conjunction with the silicon neuron (Mahowald and Douglas, 1991).

2. Methods

The postsynaptic current is modeled by a current mirror integrator with adjustable gain. It consists of two transistors (T3, T4) and a capacitance (Ci) (see Fig. 1A and B, the grey box labeled *EPSC modeling*). In the following we explain how the circuit operates.

We first study the behavior of the circuit without the capacitance Ci. The two transistors (T3, T4)—of which T3 is diode connected—form a simple current mirror (Mead, 1989, p. 39). The current through T4 is a copy of the current through T3, hence the name *current mirror*. A pulsed input current will result in a pulsed output current. Transistor T4 acts like a current source and dumps the current on V_{m}, the membrane

potential node. The gain of the current mirror is set by the difference between the two voltage sources EION and TAU. A pulsed input current will result in a scaled pulsed output current.

A current mirror with a capacitance (C_i) is a current mirror integrator. The capacitance sets the dynamics of the mirrored current. A pulsed input current will result in the following output: during the pulse the output current will increase roughly sigmoidally; at the end of the pulse the output will decrease like 1/time.

By changing the gain of the current mirror we can modulate the rise and decay time constant of the output current. Figure 1C shows qualitatively the EPSC dynamics for two values of TAU. They are roughly similar to dynamics of EPSC models, which show a fast increase and a slower decrease in current (Johnston and Wu, 1995).

The parameter EION is a fixed voltage and can be seen as the reversal potential of the ion.

2.1. The AMPA Conductance

Neurons communicate with each other by spikes propagating on axons. In silicon networks (Deiss et al., 1998), communication between neurons is done through digital voltage pulses. At each synapse, this digital pulse has to be converted into analog currents suitable for computation in silicon neurons. In Fig. 1A and B transistors T1 and T2 carry out this conversion and can be viewed as the presynaptic terminal.

Transistor T1 is driven by the presynaptic voltage pulse (SPK). Therefore, T1 works like a switch. This step is labeled *input*. We scale down the digital current to an analog current (IWGT) by applying an analog voltage (WGT) to the gate of T2. WGT represents the weight of the synaptic conductance. That part of the circuit is labeled with *strength*. The current IWGT then goes through the current mirror integrator.

2.2. The NMDA Conductance

To include a voltage dependence in our synaptic scheme, we choose a differential pair (Mead, 1989, p. 67). This device generates an output current that is proportional to its input voltage difference. The circuit consists of three transistors: a bias transistor T2a that sets the maximum current (bias current); and two transistors T2b and T2c whose gate voltages determine the ratio of the currents that flow through the two transistors (labeled *voltage dependence*).

The bias transistor T2a represents the weight as does T2 in the AMPA circuit. The membrane potential (V_m) at T2c is compared against a fixed reference voltage (REF) at T2b. If V_{m} is high during the pulse input on T1, more current goes through transistor T2c. This current is used for the EPSC.

3. Results

A chip of approximately 2×2 mm^2 was fabricated using a standard 2 μm CMOS technology. Transistors of the synaptic circuits are 6μ wide and 4μ long. The capacitance C_i is about 0.45 pF. The remaining figures (2–6) show recordings from that chip.

As a passive membrane model we use a follower integrator (Mead, 1989, chap. 9), whose output represents the membrane voltage. The follower integrator is a rough approximation to a RC circuit, and we used it already for the silicon neuron (Rasche et al., 1998). The resistance of the follower integrator can be set by the transconductance of the amplifier. The synaptic currents (IAMPA and INMDA) are sourced into the capacitance of the follower integrator.

Examples of EPSP dynamics of our synaptic aVLSI conductances are illustrated in Fig. 2. Responses show the two possible extreme dynamics (a and b) that are determined by the current mirror integrator. Decay times are between around 20 and 30 ms. The constant decay is due to the large signal input of the follower integrator.

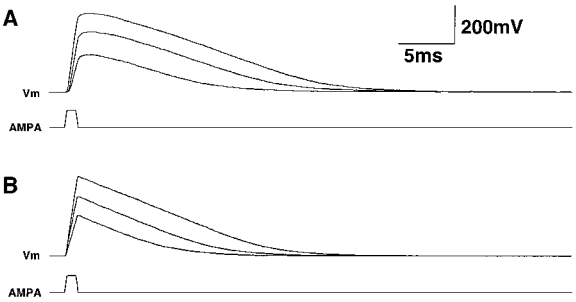

Figure 2. These and following figures show recordings from a fabricated chip. Response of the membrane voltage (V_{m}) after stimulation of a silicon AMPA conductance by a presynaptic spike (AMPA). Two different EPSP dynamics (a and b) for three different weights are shown. EPSP maximum amplitudes are 200, 300, and 400 mV. A: TAU = 4.08 V, WGTS = 0.515, 0.53 and 0.547 V, respectively. B: TAU = 4.3 V, WGTS = 0.811, 0.823 and 0.834 V, respectively. For all the plots shown, we chose the following parameter values: presynaptic pulse width of 1 ms, resting potential = 1.2 V, EION = 4.0 V.

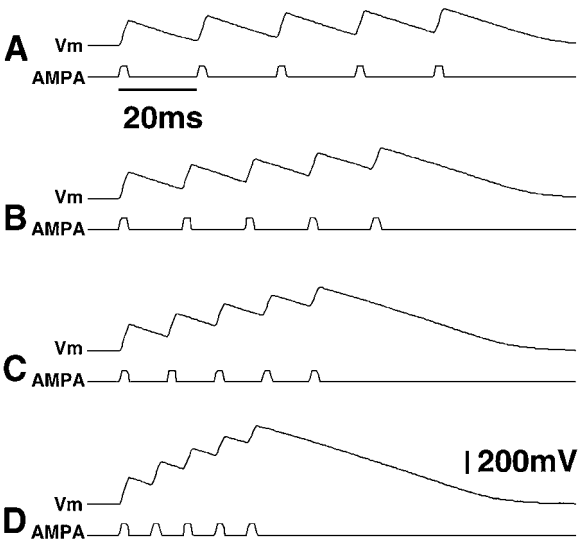

Figure 3. Response of V_m after stimulation of a silicon AMPA conductance by a presynaptic burst of spikes (AMPA). The burst consists of a sequence of five spikes with various interval lengths: A: 10 ms, B: 8 ms, C: 6 ms, D: 4 ms. A single EPSP has an amplitude of 200 mV. Parameter values: TAU = 4.3 V, WGT = 0.811 V.

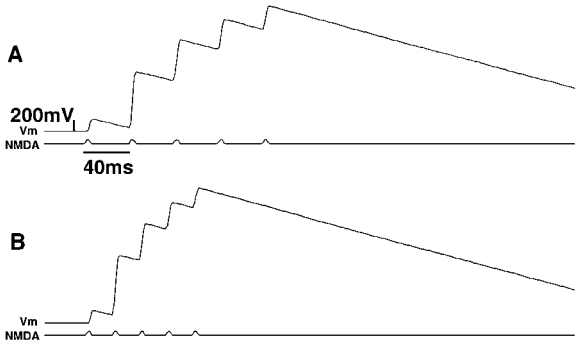

Figure 4. Response of V_m after stimulation of a silicon NMDA conductance by a presynaptic burst of spikes (NMDA). As before, the burst consists of a sequence of five spikes with various interval lengths: A: 10 ms, B: 4 ms. The first EPSP has an amplitude of 200 mV as the EPSP amplitude of Fig. 3. The amplitudes of the second and third EPSP show the amplifying effect of the NMDA conductance. Parameter values: REF = 1.3 V, TAU = 4.08 V, WGT = 0.564 V.

Figure 3 demonstrates the summation of V_m due to the AMPA conductances in response to a burst of spikes. Summation is initially linear and shows later signs of sublinear summation due to the decreased voltage difference (V_m-EION) across transistor T4. The difference is equivalent to the driving force ($V - E$) in biological membranes.

The effect of the NMDA conductance on V_m is demonstrated in Fig. 4. Presynaptic stimulation occurs

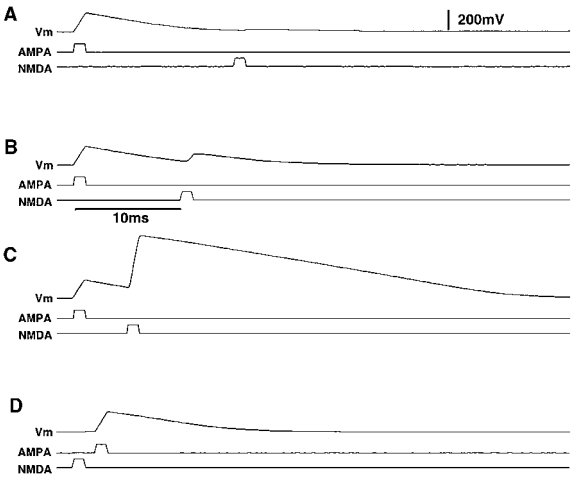

Figure 5. Demonstration of the amplifying effect of the NMDA conductance in conjunction with the AMPA conductance. A–C: An AMPA stimulation (upper pulse) is followed by a NMDA stimulation (lower pulse) with decreasing interval. A: Interval 15 ms. The voltage dependence does not have a significant effect yet. Here, the weight of the NMDA is smaller than in the experiment in Fig. 3 and a single NMDA EPSP can hardly be seen. B: Interval 10 ms. First signs of voltage dependence emerge. C: Interval 5 ms; voltage dependence in its full extent. In contrast: D: The NMDA conductance stimulation is followed by an AMPA conductance stimulation. The preceding NMDA EPSP can hardly be seen. Parameter values: NMDA WGT = 0.538 V. All other parameter values are the same as for Figs. 3 and 4.

as before by a burst of spikes. A single EPSP has the same amplitude as in the previous experiment and allows us to directly compare the integration of V_m with the AMPA summation in Fig. 3. The second EPSP amplitude is larger than the corresponding second EPSP amplitude in Fig. 3. The same applies for the third EPSP. The fourth and fifth EPSP amplitudes begin to saturate. This saturation behavior is again due to the decrease of the voltage difference (V_m-EION) across transistor T4.

Figure 5 shows the amplifying effect of the NMDA conductance in conjunction with an AMPA EPSP. In Fig. 5A to C, the AMPA conductance was first activated and then the NMDA conductance was stimulated with decreasing inter-stimulation interval. In Fig. 5A, the voltage-dependent NMDA conductance has hardly any effect. As the interval decreases, the NMDA conductance turns on and a larger EPSP amplitude is seen. In Fig. 5D the stimulation order is reversed. The NMDA conductance is now ineffective.

In Fig. 6, we demonstrate the operation of the synaptic conductances in conjunction with the silicon neuron. The operation of this neuron (without synapses) is

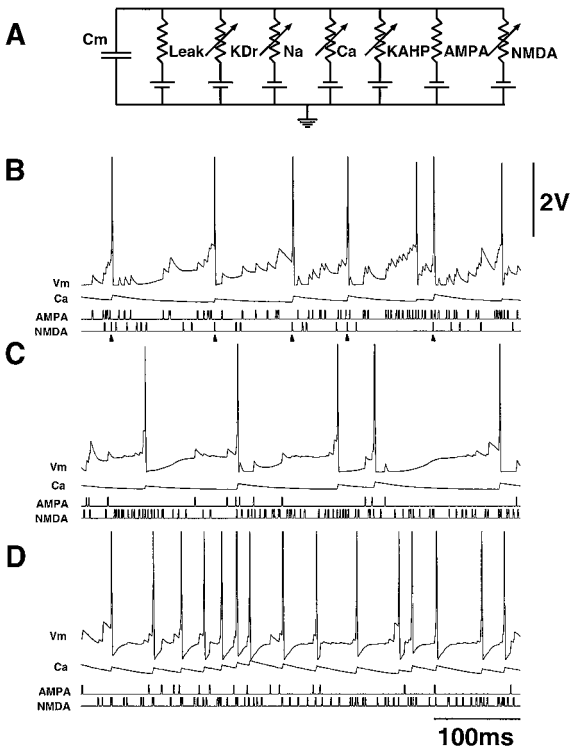

Figure 6. A compartmental representation of the somatic silicon neuron. The conductances in this soma model are Leak (leakage conductance), KDr (delayed rectifier), Na (sodium conductance), Ca (high-threshold conductance), KAHP (after-hyperpolarizing potassium conductance). B–D: The silicon neuron's response (Ca: intracellular calcium concentration) to presynaptic AMPA and NMDA bombardment. B: Stimulation of the AMPA conductance occurs at a mean frequency of 200 Hz, stimulation of the NMDA conductance at 50 Hz. The intervals of the synaptic spike stimuli are Poisson distributed. The NMDA conductance sometimes acts as an coincidence detector: see arrows on NMDA stimulation trace. C: The two synaptic stimulation frequency values are switched. The resulting spike frequency is lower than in B. After-spike hyperpolarization prevents the NMDA conductance from turning on. D: Stimulation as in C with KAHP conductance turned off. After-spike hyperpolarization is not prominent anymore and the membrane potential repolarizes faster. Synaptic parameter values: as for Figs. 3 and 4. Relevant neuron parameters: resting potential = 1.2 V, spiking threshold = 1.8 V, sodium reversal potential = 4.0 V, potassium reversal potential = 1.0 V.

described in (Rasche et al., 1998). Figure 6A shows a compartmental model of the silicon neuron.

In Fig. 6B–D, we show 500 ms recordings of V_m and Ca, during synaptic bombardment of the AMPA and NMDA conductances. Ca represents the intracellular calcium concentration of a nerve cell and is given as a voltage. In Fig. 6B, the AMPA conductance was stimulated at a mean frequency of 200 Hz, the NMDA conductance was stimulated at 50 Hz. The spike train shows seven spikes of which five were elicited by a NMDA stimulation. These five NMDA stimulations are indicated by the arrows below the NMDA stimulation trace.

In Fig. 6C, the AMPA and NMDA stimulation frequencies were interchanged. Since the NMDA conductance was stimulated at a higher frequency, one might expect an increased spike frequency from the amplifying effect of the NMDA. But the spike frequency does not increase. The reason for this behavior is that once the membrane potential is hyperpolarized after a spike, the NMDA cannot inject any current at low membrane voltages. In Fig. 6D, the synapses were stimulated as in Fig. 6C, but the KAHP conductance (responsible for spike frequency adaptation via calcium concentration) was turned off. The membrane potential recovers faster, and hence, we observe an increased spike frequency.

4. Discussion

Our approach in designing analog circuits that capture neuronal computation is phenomenologically based. If a circuit shows a reasonable biological approximation in simulation and fulfils the important design constraints (less silicon area, few parameters), we implement it. The synaptic conductance circuits presented here are one example of this philosophy.

On the other hand, an accurate simulation of for example an alpha function in silicon is possible (Dupeyron et al., 1996), but such a circuit needs more parameters (and therefore more tuning) and silicon area.

Here we have presented a simple silicon model of the EPSC: a current mirror integrator with adjustable gain suffices to approximate the dynamics of an EPSC caused by an AMPA or NMDA conductance. We have shown the effect of parameter TAU in Fig 2. Its effect of modulating the decay time constant is not as prominent, as we originally expected, because the decay times for the EPSC are too short. However, it can be useful for adjusting the dynamics of the EPSP when the neuron operates in a network. The voltage dependence of a NMDA conductance can be simulated by a differential pair.

In terms of neuromorphic systems constraints we achieved two important goals. First, the circuits are compact: the AMPA conductance circuit consists of only four transistors and a capacitance. The NMDA conductance circuit consists of two extra transistors. This small number of transistors allows many synapses to be implemented on a single chip.

Second, the operation of the conductances is set by only few parameters. Apart from the weight parameter, the silicon AMPA conductance circuit needs a single parameter (TAU) to adjust the EPSP dynamics. The silicon NMDA conductance needs only an additional parameter (REF) to set the voltage dependence.

In the silicon NMDA conductance, the voltage dependence is effective during the presynaptic pulse application on T1; otherwise the differential pair is turned off. Hence, the amplifying effect of the NMDA conductance acts only during the presynaptic pulse (1 ms). For that reason the NMDA EPSP amplitude in Fig. 5D is low. If an AMPA stimulation follows right after a NMDA stimulation, no amplification occurs. A more realistic NMDA conductance should show such a amplification during the entire EPSC, which lasts several milliseconds.

By moving the reference voltage REF, the voltage-sensitive range can be shifted to a desired level. In Fig. 5 the reference voltage is low, so that a single AMPA EPSP can elicit a NMDA response. If the reference voltage is high, a higher membrane voltage is required—for example, several summed AMPA EPSPs—to evoke a NMDA EPSP.

In our experiments in Fig. 6, we have a somatic model with an NMDA conductance. This model is not completely biologically plausible, but we demonstrate the successful integration of synaptic conductances with the silicon neuron (Mahowald and Douglas, 1991; Rasche et al., 1998). Figure 6B shows that the lower-stimulated NMDA conductance can occasionally act as a coincidence detector (König et al., 1996). The membrane potential wanders between the resting potential and the spiking threshold, and some of the NMDA stimulations (see arrows) cause the membrane voltage to jump directly above the spiking threshold. The increased and decreased spike frequency in the experiments in Fig. 6C and D can be explained by the presence and absence of the KAHP conductance. In Fig. 6C, the membrane potential stays hyperpolarized for a while after a spike because the KAHP current is turned on as long as the calcium concentration is high (Rasche et al., 1998). During this hyperpolarization, stimulation of the NMDA conductance causes no EPSP since the membrane potential is too low. Once the membrane potential is repolarized, the NMDA conductance amplifies again. In Fig. 6D, stimulation is the same as in Fig. 6C, but the KAHP conductance was turned off. As a result, the membrane potential repolarizes faster after a spike than in the experiment in Fig. 6C. Hence, the NMDA conductance acts earlier, and the frequency increases.

We have shown the performance of our circuit as it stands at the moment. However, the NMDA circuit needs to be improved to overcome the deficiency seen in Fig. 6D and discussed in this section. We hope to report on a improved circuit and compare it with biological data in a later paper.

The synaptic conductances have already been successfully used in other applications. In Häfliger and Rasche (1999), the weight value on T2 of the AMPA conductance can be changed according to an on-chip learning rule (Häfliger and Mahowald, 1999) to emulate LTP and LTD.

A silicon dendrite (for example, Elias, 1993) endowed with these synaptic conductances—in particular the NMDA conductance—could give rise to multiplicative-like operations in a dendritic tree. In computer modeling various models have been already proposed (Mel, 1992a, 1992b; Durbin and Rumelhart, 1989). For a silicon realization a suitable model has to be found.

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